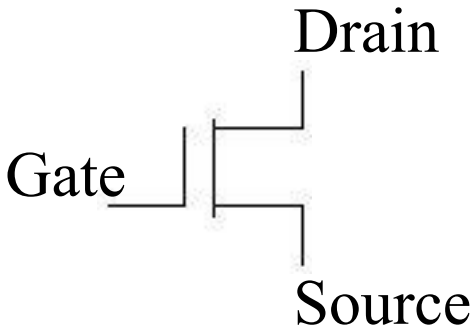
FIELD EFFECT TRANSISTORS
(FET)

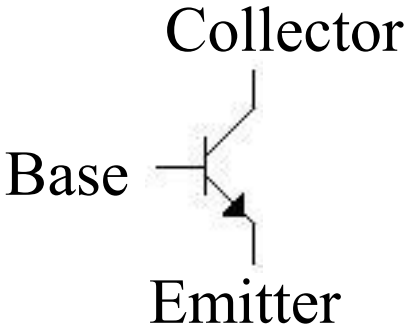
Dr. Vivek Ambalkar

FET x BJT (NPN)



FET

- ✓ 3 terminal device
- ✓ Channel e^- current from source to drain controlled by the electric field generated by the gate
- ✓ Extremely high input impedance for base



BJT

- ✓ 3 terminal device emitter to collector e^- current controlled by the current injected into the base

Types of FETs

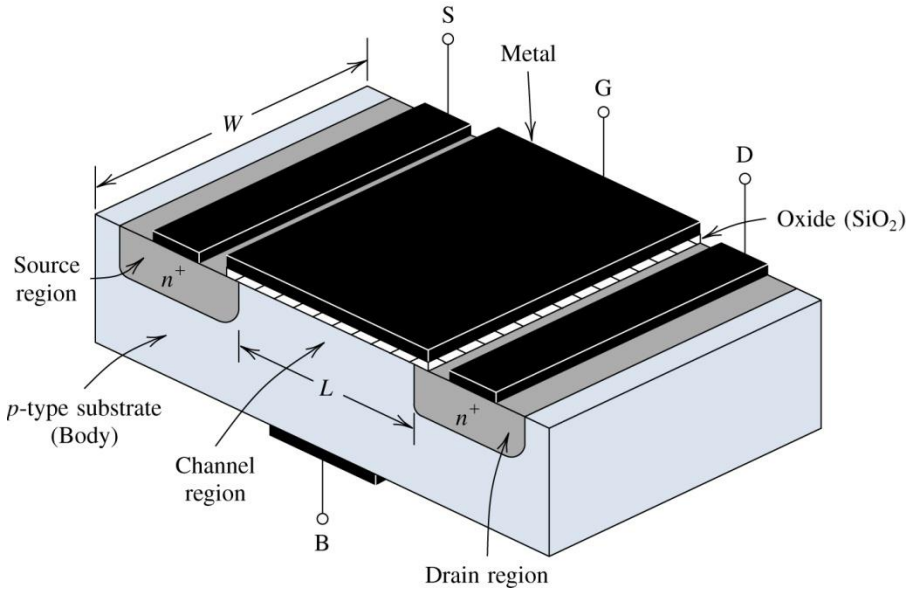
- In addition to carrier type (N or P channel), there are differences in how the control element is constructed (Junction x Insulated) and those devices must be used differently

Depletion mode junction FETs (JFET)
- npn
- pnp

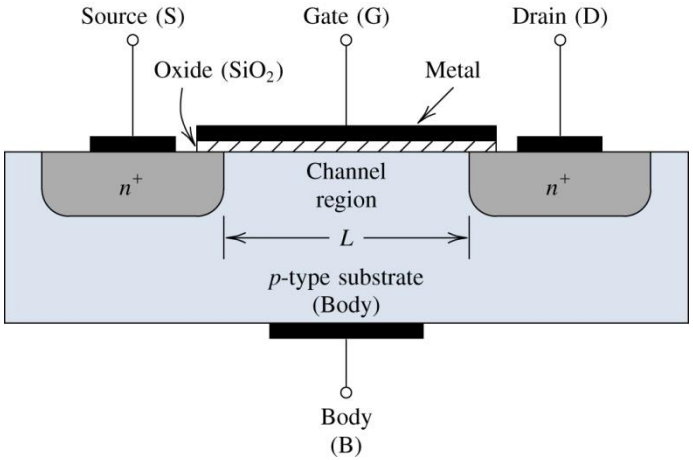
Metal oxide semi-conductor FET (MOSFET)
- npn
- pnp

  – depletion/enhancement mode
  – enhancement mode

(insulated gate FETs, IGFETs, are the same as MOSFETs)

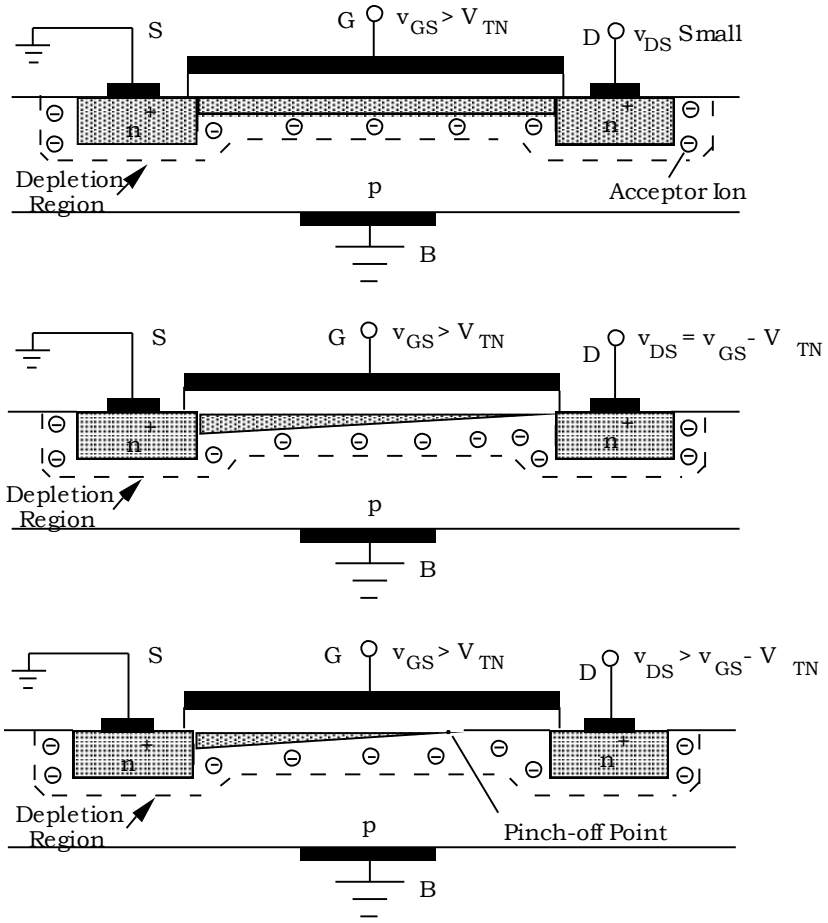


(a)



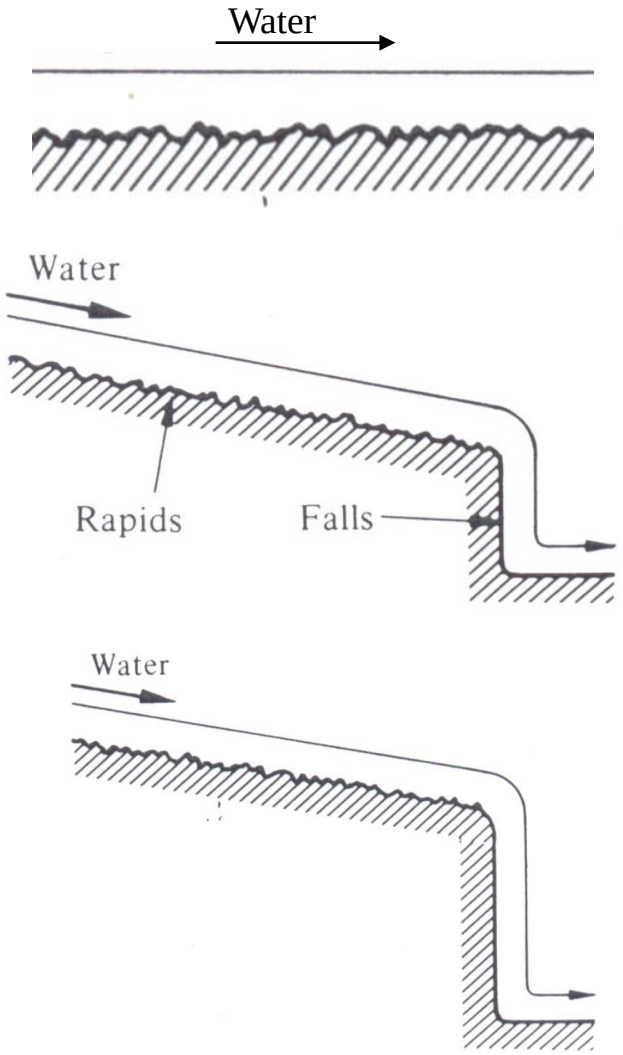
(b)

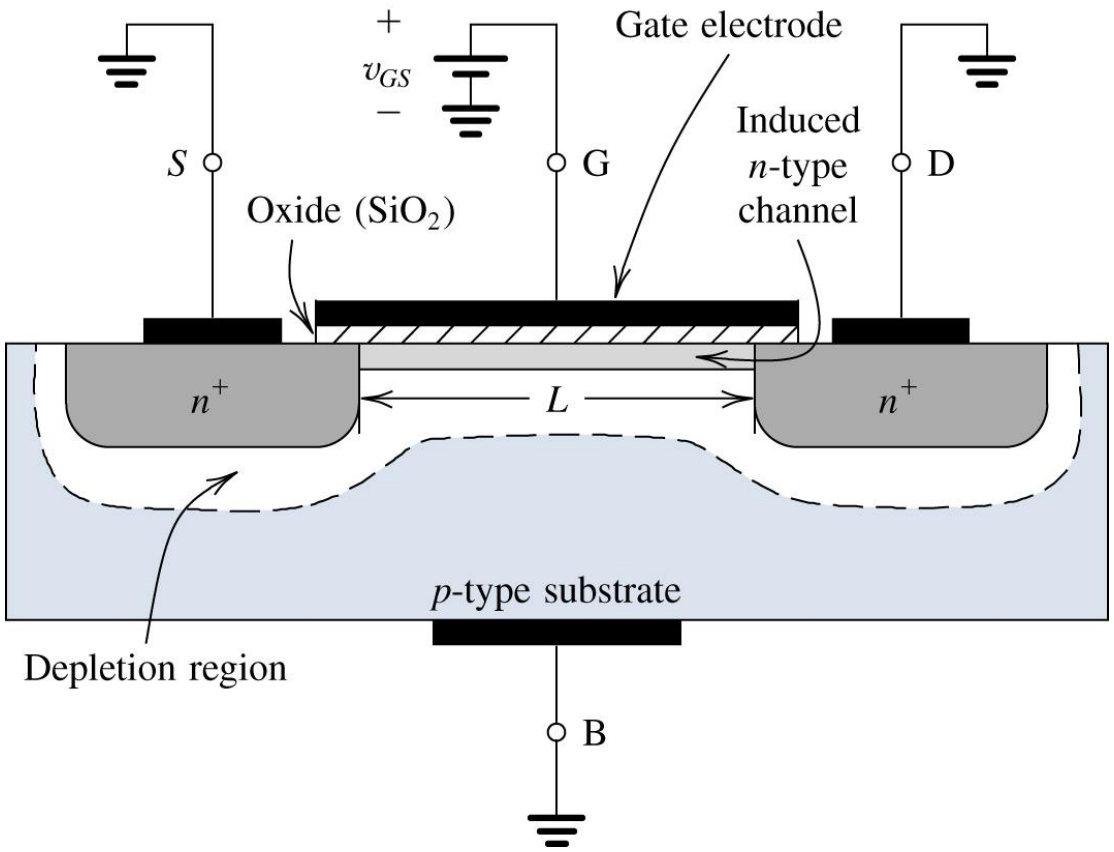
Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 1 to 10 μm, W = 2 to 500 μm, and the thickness of the oxide layer is in the range of 0.02 to 0.1 μm.



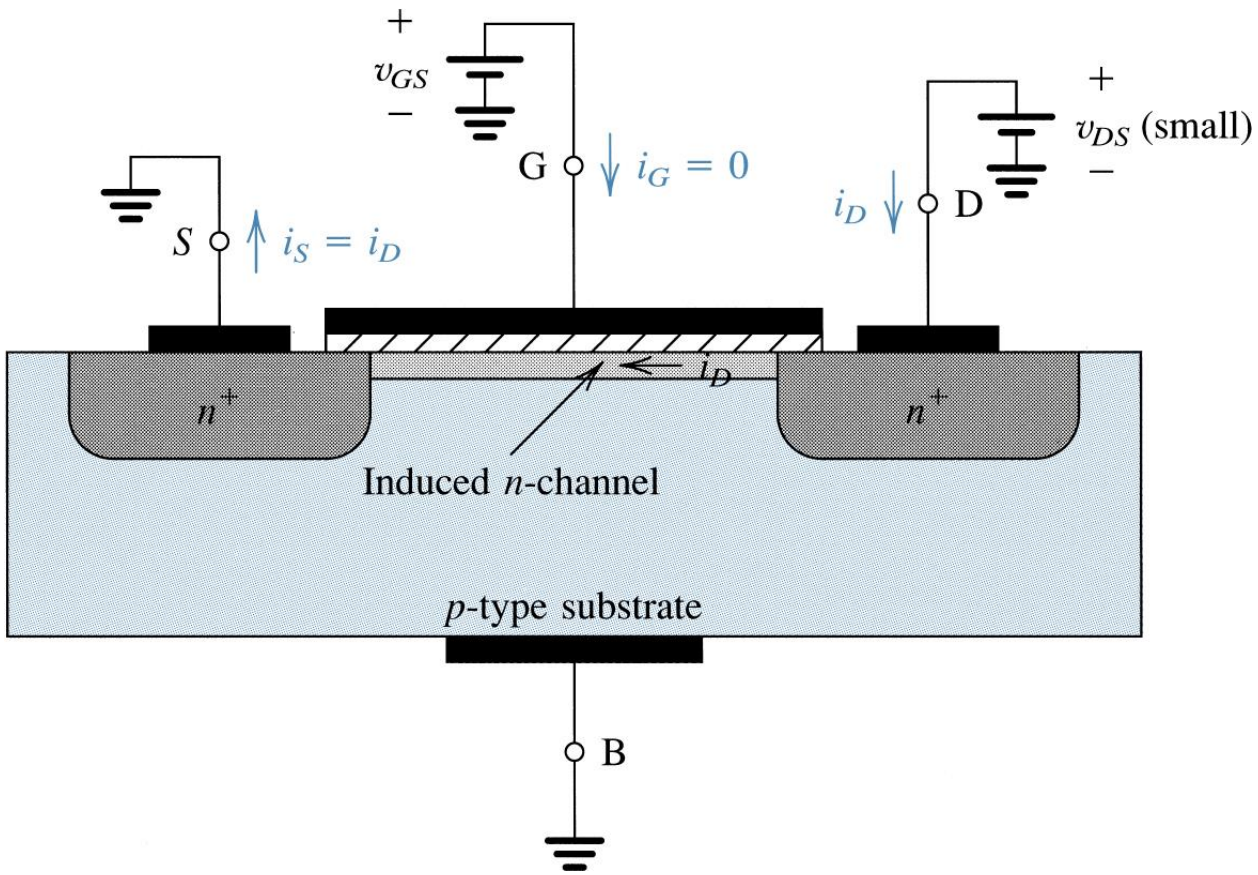
(a) MOSFET in the linear region
(b) MOSFET with channel just pinched off at the drain.
(c) Channel pinch off for $v_{DS} > v_{GS} - V_{TN}$

Waterfalls analogy





The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

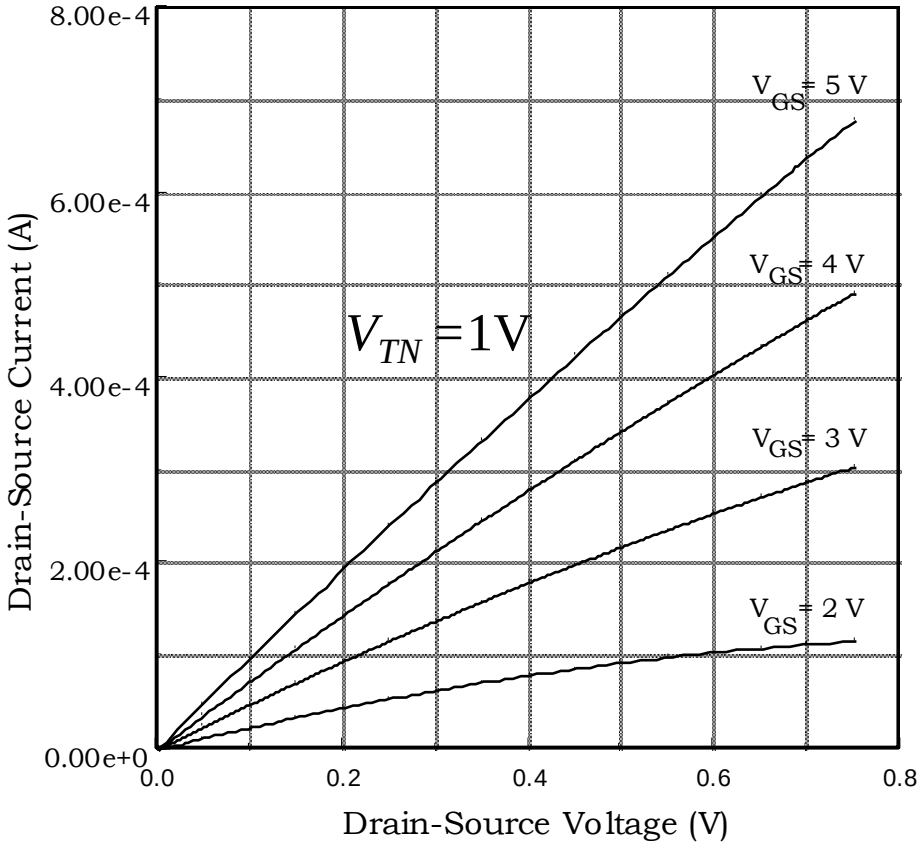


An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a conductance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and this i_D is proportional to $(v_{GS} - V_t)\, v_{DS}$. Note that the depletion region is not shown (for simplicity).

$$i_D = \mu_n C_{OX} \frac{W}{L}\left[(v_{GS} - V_{tn})v_{DS} - \frac{v_{DS}^{\ 2}}{2}\right]$$

$$v_{GS} \geq V_{tn}$$

$$0 \leq v_{DS} \leq v_{DSSAT} = v_{GS} - V_{tn}$$



NMOS i-v characteristics in the linear region (V_{SB} = 0)

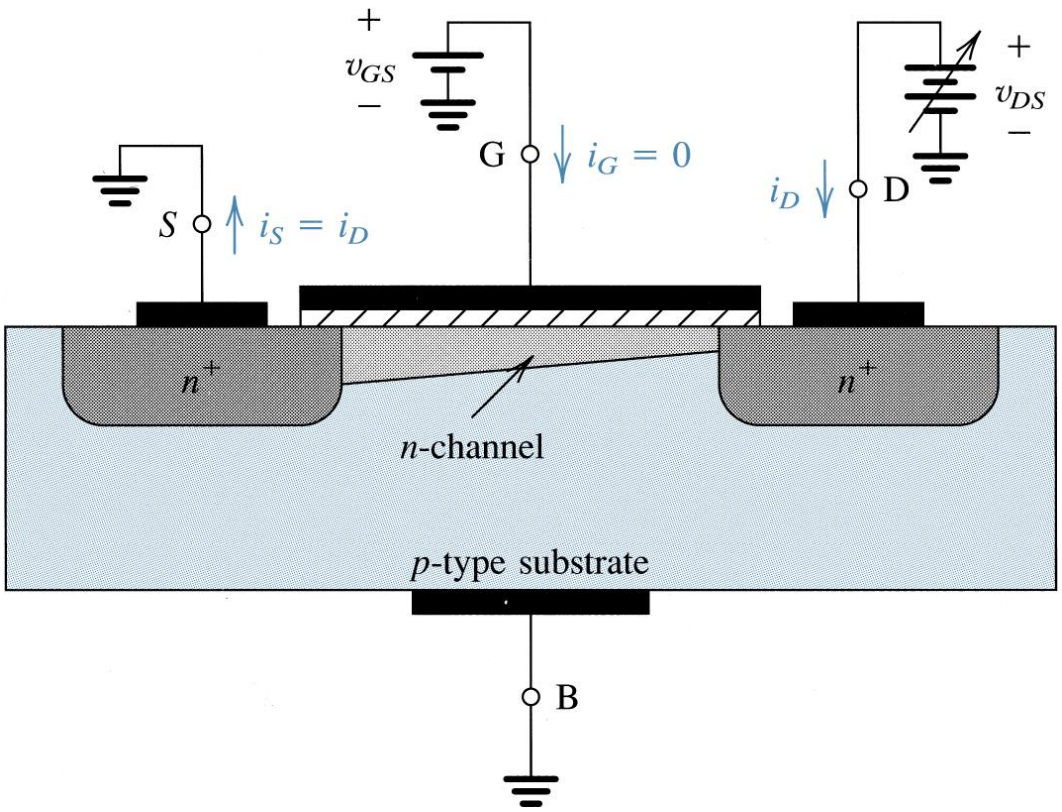
$$k_n' = \mu_n C_{OX}$$

small v_{DS}

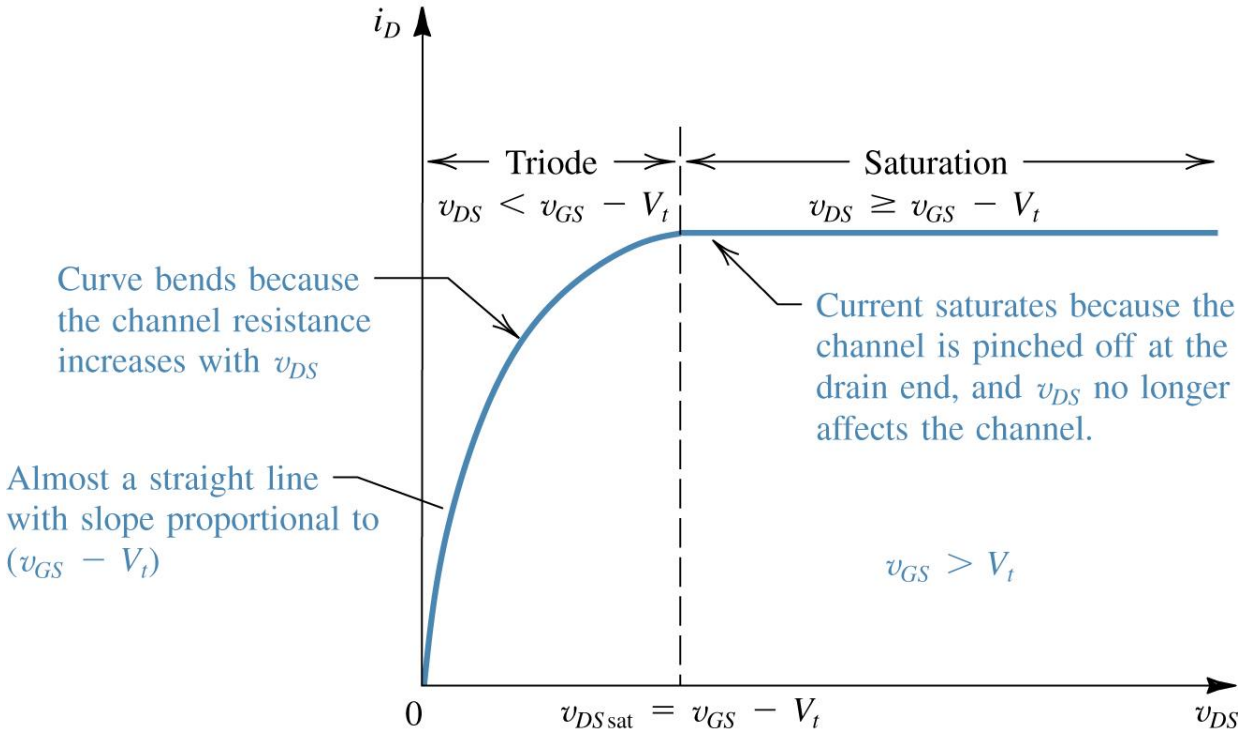
$$i_D = k_n' \frac{W}{L}(v_{GS} - V_{tn})v_{DS}$$

$$\frac{di_D}{dv_{DS}} = k_n' \frac{W}{L}(v_{GS} - V_{tn})$$

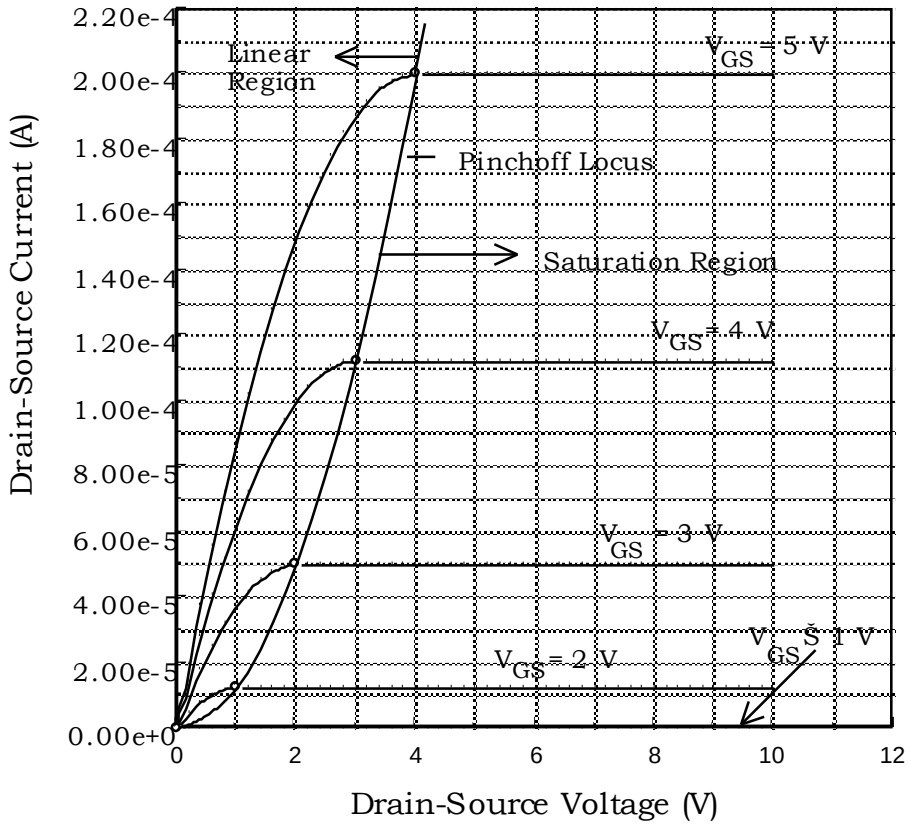
Linear Region (*small* v_{DS})



Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.



The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.



$$i_D \approx 0 \quad for \quad v_{GS} \le V_{tn}$$

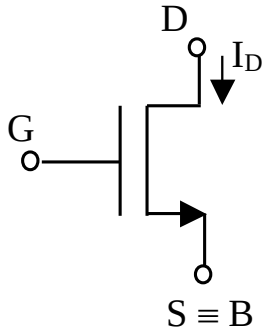
$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_{tn})v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$for \begin{cases} v_{GS} \ge V_{tn} \\ v_{DS} \le v_{DS_{SAT}} = v_{GS} - V_{tn} \end{cases}$$

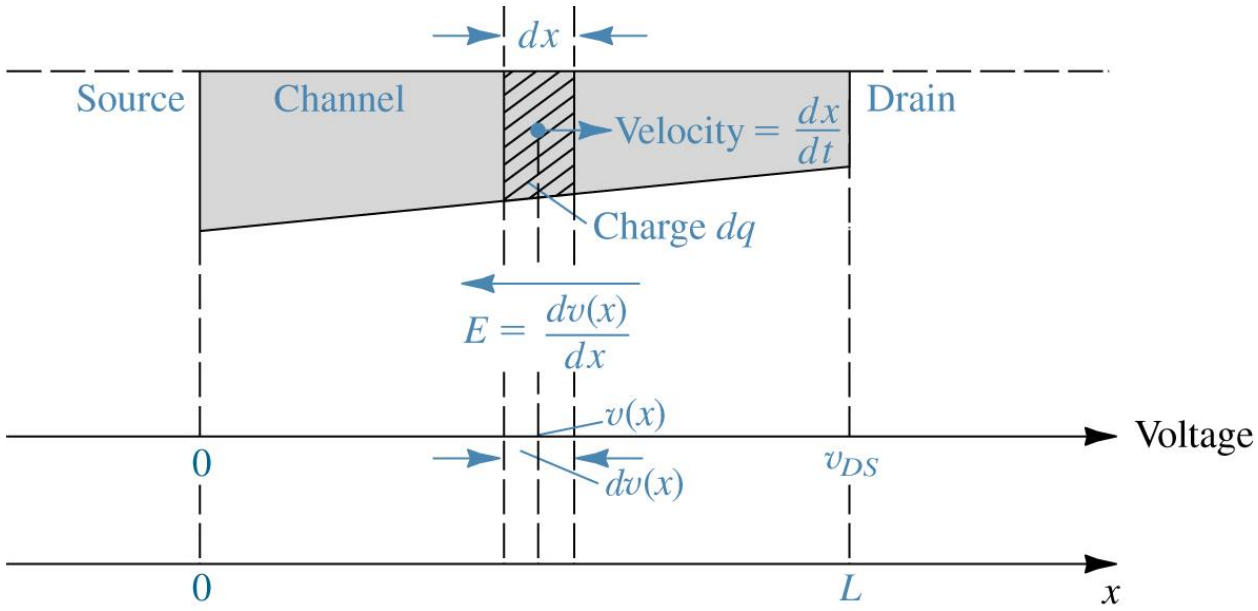
$$i_D = \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_{tn})^2$$

$$for \begin{cases} v_{GS} \ge V_{tn} \\ v_{DS} \ge v_{DS_{SAT}} = v_{GS} - V_{tn} \end{cases}$$

Output characteristics
for an NMOS transistor with
V_{tn} = 1 V and $k'_n\,(W/L)$= 25 x 10^{-6} A/V^2

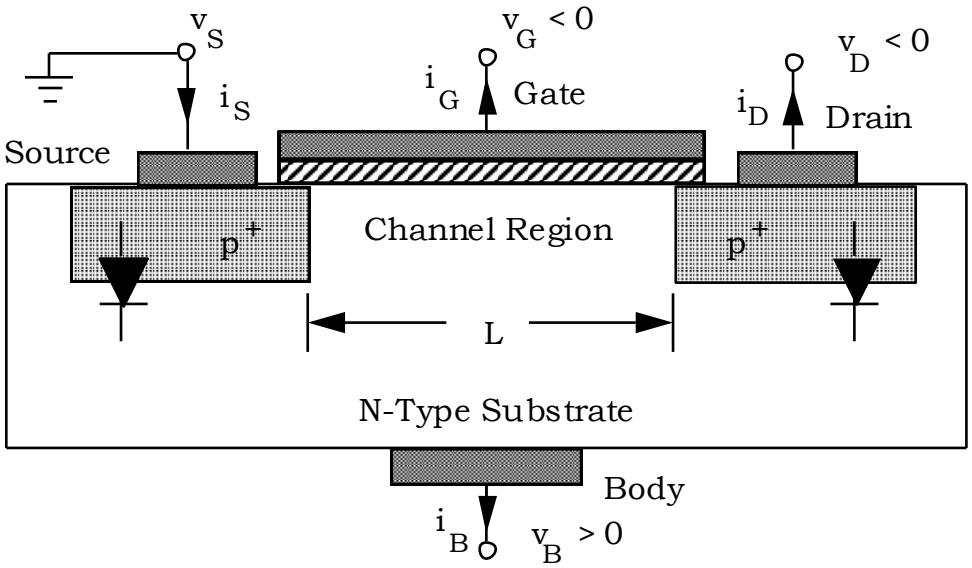


$$v_D \ge v_S$$

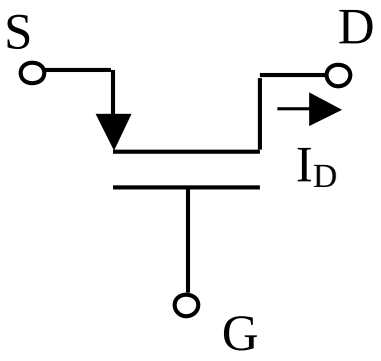


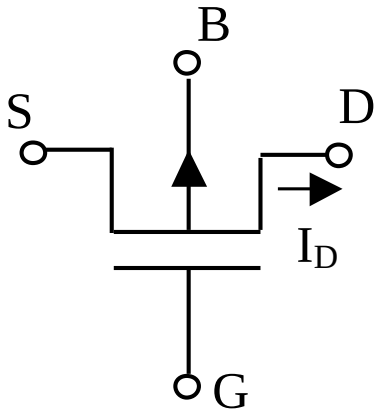
Derivation of the i_D - v_{DS} characteristic of the NMOS transistor.

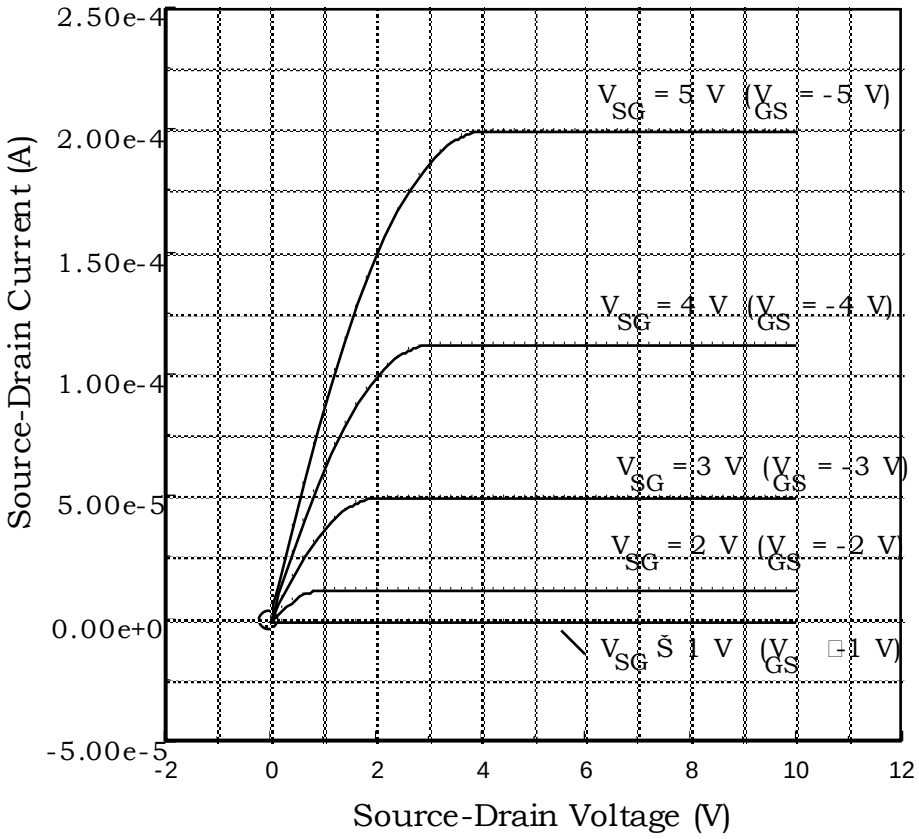
The PMOS Transistor



Cross section of an enhancement-mode PMOS transistor







Output characteristics for a PMOS transistor with V_{tp} = -1V and k'_P (W/L)= 25 x 10^{-6} A/V^2

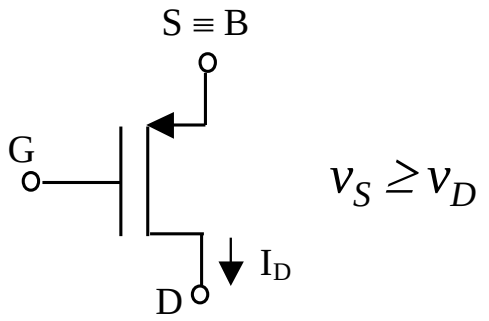
$$i_D \approx 0 \quad for \quad v_{GS} \geq V_{tp}$$

$$i_D = k'_p \frac{W}{L}\left[\left(v_{GS} - V_{tp}\right)v_{DS} - \frac{v_{DS}^{\,2}}{2}\right]$$

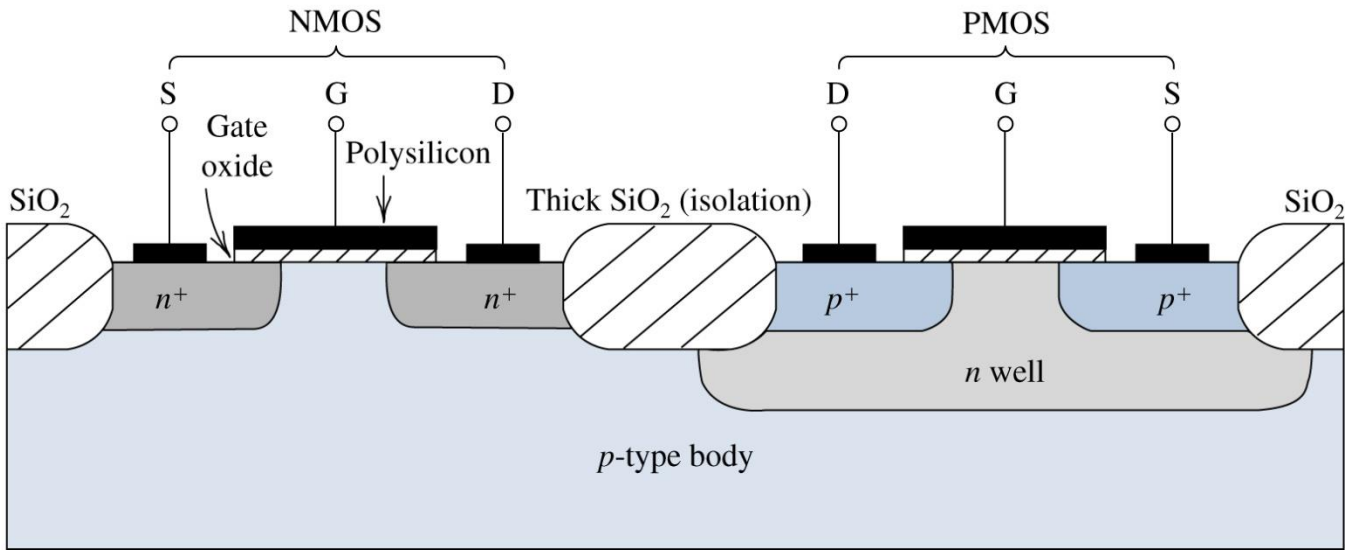
$$for \begin{cases} v_{GS} \leq V_{tp} \\ v_{DS} \geq v_{DS_{SAT}} = v_{GS} - V_{tp} \end{cases}$$

$$i_D = \frac{k'_p}{2}\frac{W}{L}\left(v_{GS} - V_{tp}\right)^2$$

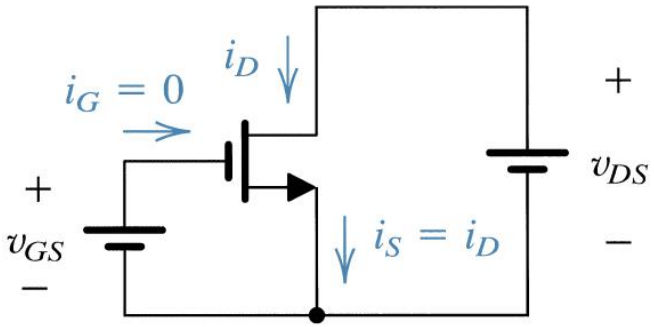
$$for \begin{cases} v_{GS} \leq V_{tp} \\ v_{DS} \leq v_{DS_{SAT}} = v_{GS} - V_{tp} \end{cases}$$



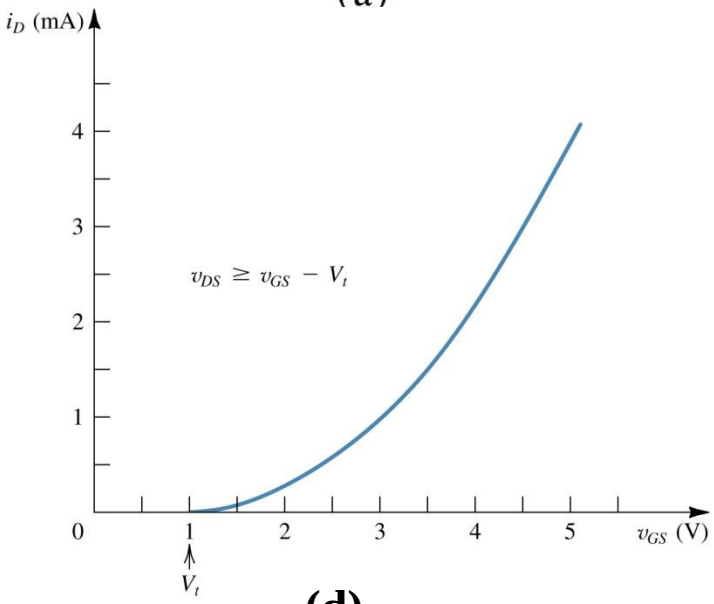
$$v_S \geq v_D$$



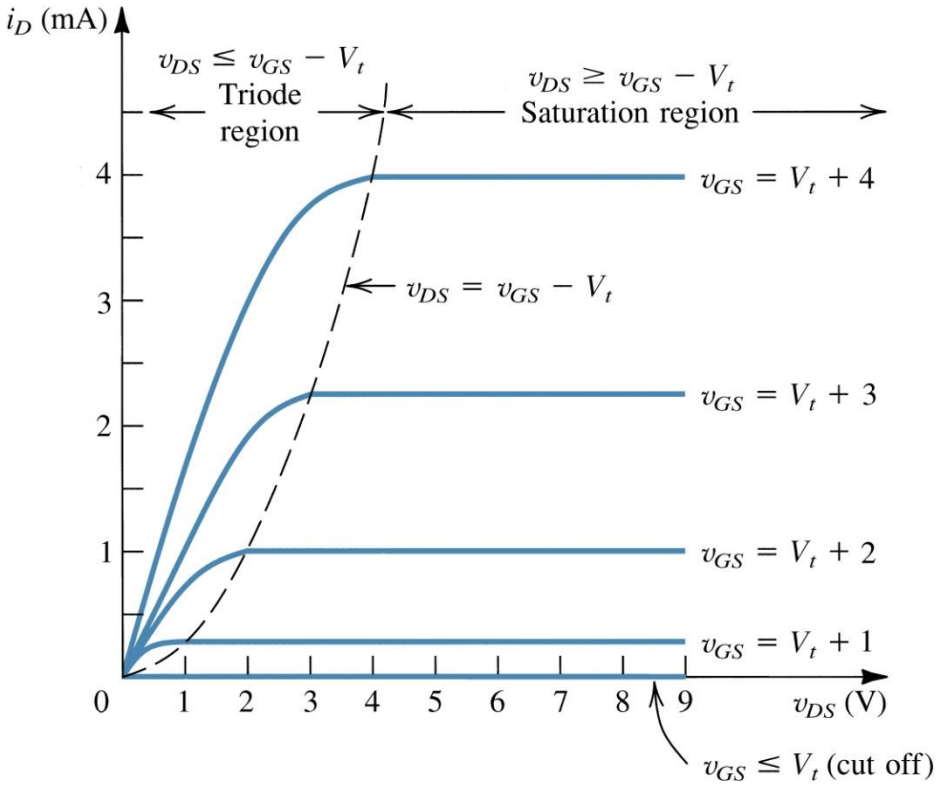
Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well.



(a)



(d)



(a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated. **(b)**The i_D - v_{DS} characteristics for a device with V_t = 1 V and $k'_n(W/L)$ = 0.5 mA/V^2 **(d)** The i_D - v_{GS} characteristic for an enhancement-type NMOS transistor in saturation.

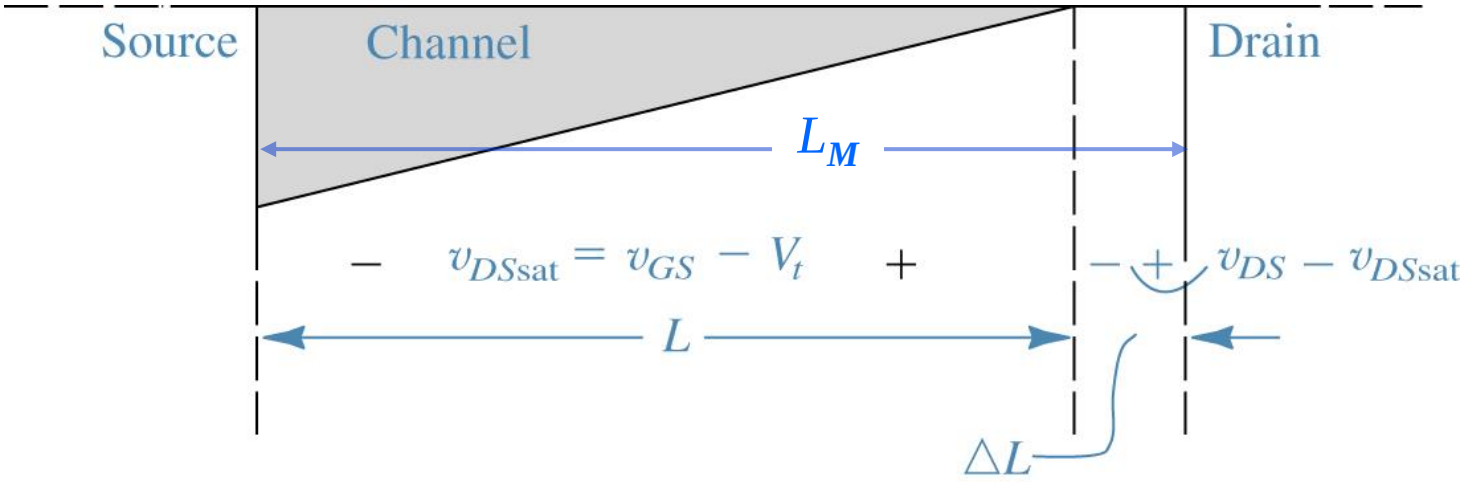
Channel Length Modulation

$$i_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(v_{GS} - V_t\right)^2 = I_{D_{SAT}} \rightarrow L = L_M$$

$$i_D = \frac{I_{D_{SAT}}}{1 - \Delta L / L_M} \cong I_{D_{SAT}}\left(1 + \Delta L / L_M\right)$$

$$\Delta L / L_M = \lambda\, v_{DS} \quad \therefore \quad \frac{1}{\lambda} = V_A \propto L$$

$$i_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(v_{GS} - V_t\right)^2\left(1 + \lambda\, v_{DS}\right)$$



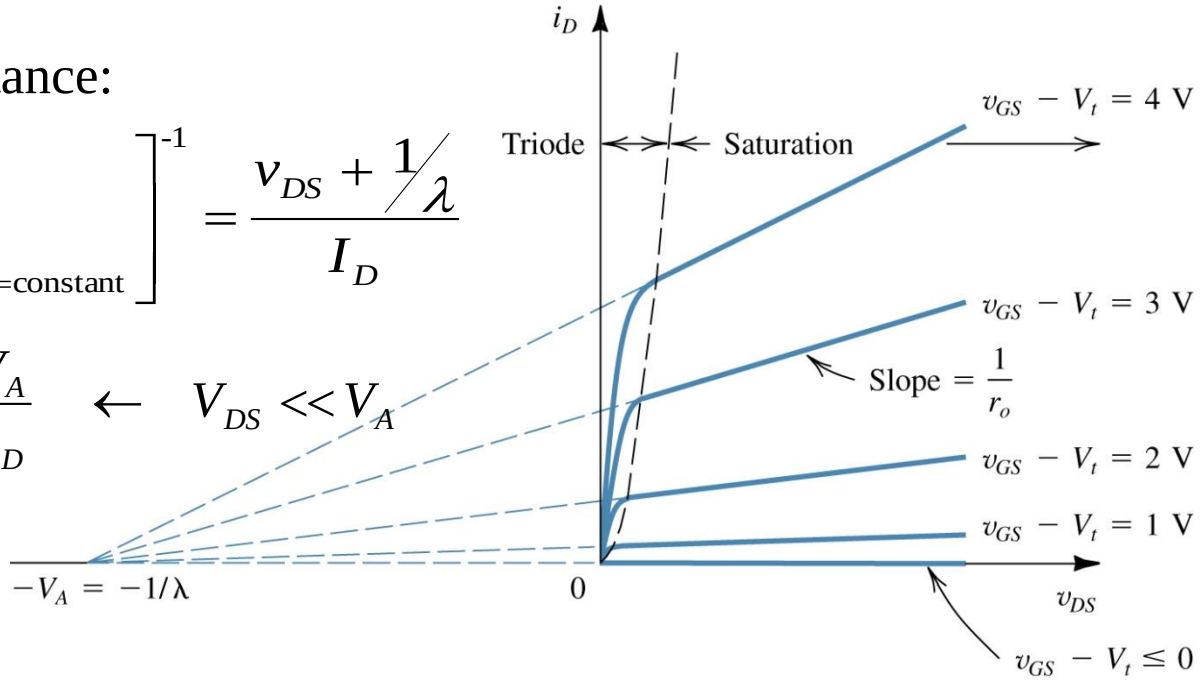
Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

$$i_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \leftarrow \text{Saturation}$$

Output Resistance:

$$r_o = \left[\left.\frac{\partial i_D}{\partial v_{DS}}\right|_{v_{GS}=\text{constant}}\right]^{-1} = \frac{v_{DS} + 1/\lambda}{I_D}$$

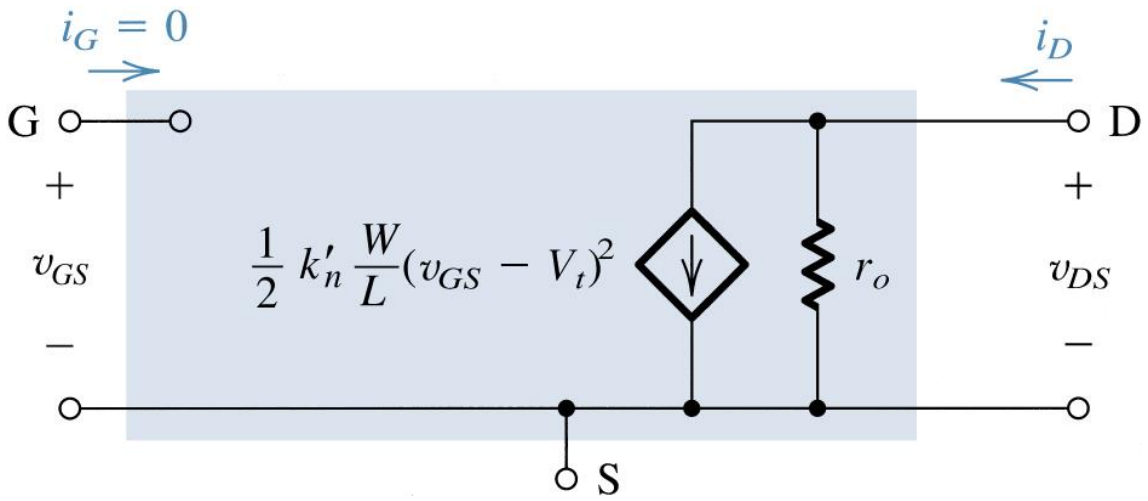
$$r_o \approx [\lambda I_D]^{-1} = \frac{V_A}{I_D} \quad \leftarrow \quad V_{DS} << V_A$$



V_A is directly proportional to L; thus two devices with the same process, and having channel lengths L_1 e L_2, will have Early voltage V_{A1} and V_{A2},.

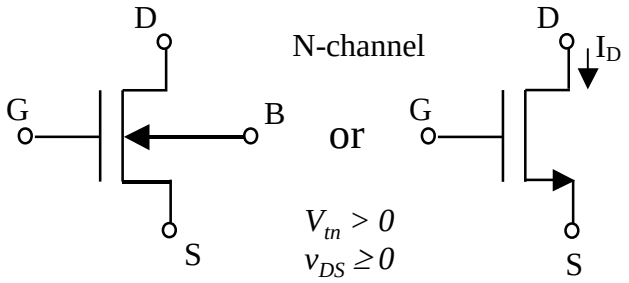
$$\frac{V_{A1}}{V_{A2}} \cong \frac{L_1}{L_2}$$

Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A is typically in the range of 30 to 200 V.



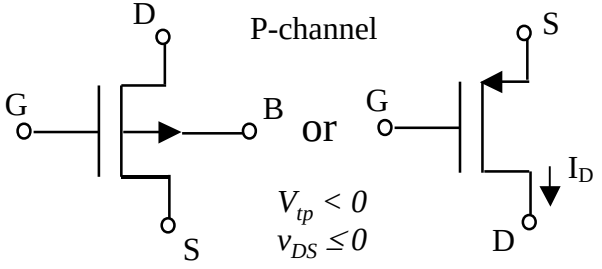
Large-signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_o. The output resistance models the linear dependence of i_D on v_{DS} and is given by $r_o \cong V_A/I_D$.

Summary of equations for the enhancement-mode MOSFET

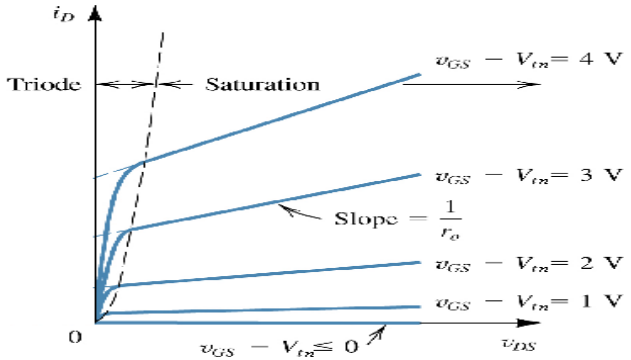


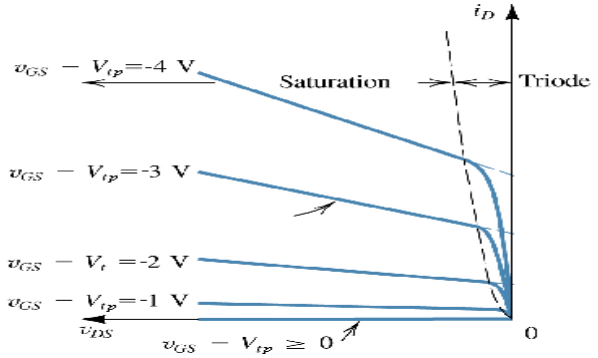
$$k_n' = \mu_n C_{ox}$$

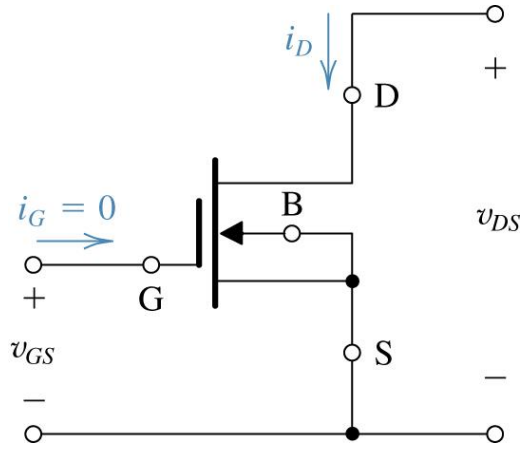
$$k_p' = \mu_p C_{ox}$$

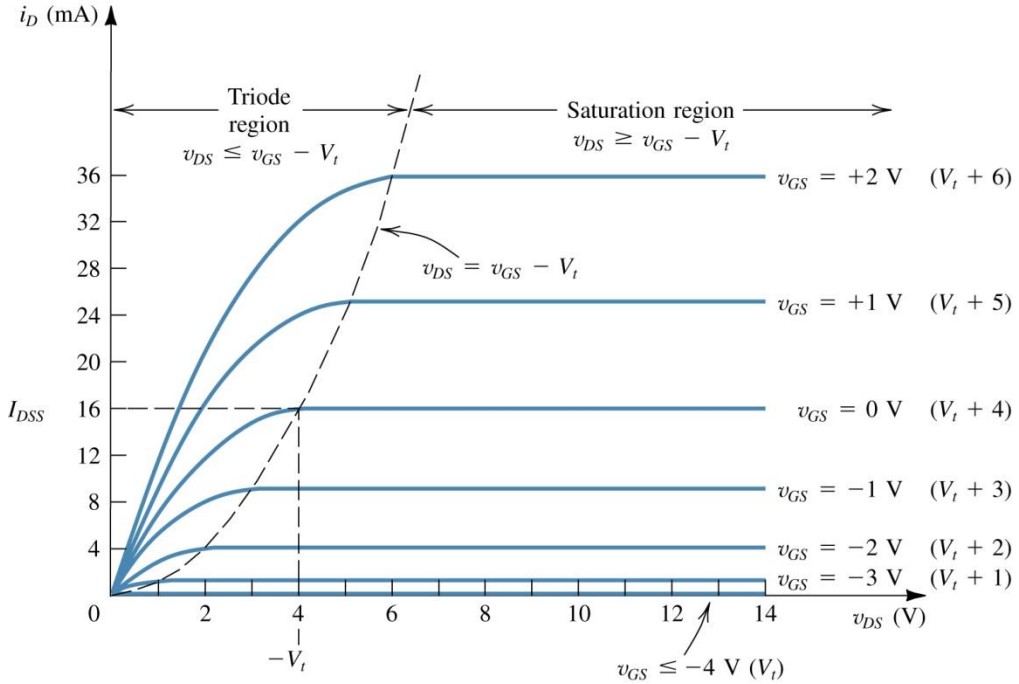


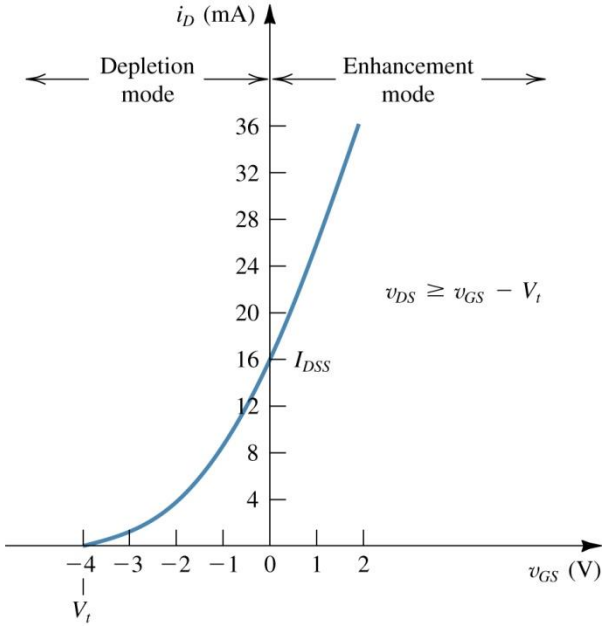
Region	N - Type	P - Type
Cutoff	$v_{GS} \leq V_{tn}$ $i_D \approx 0$	$v_{SG} \leq \lvert V_{tp} \rvert$ $i_D \approx 0$
Triodo (Linear)	$v_{GS} \geq V_{tn}$ *and* $v_{DS} \leq v_{GS} - V_{tn}$ $i_D = k_n' W/L \left[(v_{GS} - V_{tn}) v_{DS} - v_{DS}^2/2 \right]$	$v_{SG} \geq \lvert V_{tp} \rvert$ *and* $v_{SD} \leq v_{SG} - \lvert V_{tp} \rvert$ $i_D = k_p' W/L \left[(v_{SG} - \lvert V_{tp} \rvert) v_{SD} - v_{SD}^2/2 \right]$
Saturation	$v_{GS} \geq V_{tn}$ *and* $v_{DS} \geq v_{GS} - V_{tn}$ $i_D = \frac{k_n'}{2} W/L (v_{GS} - V_{tn})^2 \left(1 + \frac{V_{DS}}{\lvert V_A \rvert} \right)$	$v_{SG} \geq \lvert V_{tp} \rvert$ *and* $v_{SD} \geq v_{SG} - \lvert V_{tp} \rvert$ $i_D = \frac{k_p'}{2} W/L (v_{SG} - \lvert V_{tp} \rvert)^2 \left(1 + \frac{V_{SD}}{\lvert V_A \rvert} \right)$







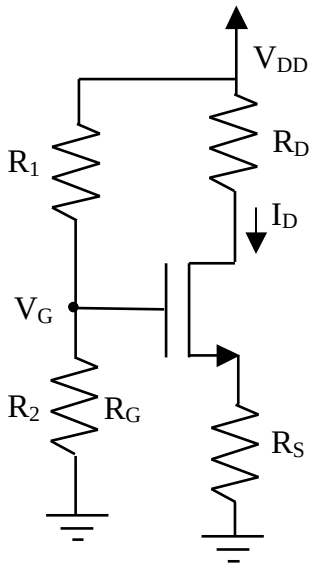




The current-voltage characteristics of a depletion-type *n*-channel MOSFET for which V_t = -4 V and $k'_n(W/L)$ = 2 mA/V^2:
(a) transistor with current and voltage polarities indicated; **(b)** the i_D - v_{DS} characteristics; **(c)** the i_D - v_{GS} characteristic in saturation.

Bias Circuits 1

- λ usually neglected ($1/\lambda = V_A \rightarrow \infty$)
- Q-point most often located in saturation for analog circuits



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \qquad V_S = R_S I_D \qquad \Rightarrow \quad V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} - R_S I_D$$

$$V_{DS} = V_{DD} - (R_D + R_S) I_D$$

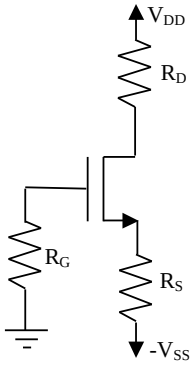
$$I_D = \frac{k_n'}{2} W/L \, (V_{GS} - V_t)^2$$ (assuming the MOSFET to be in the saturation region)

$$I_D = \frac{k_n'}{2} W/L \left[\frac{R_2}{R_1 + R_2} V_{DD} - V_t - R_S I_D \right]^2$$ (two solutions $\rightarrow$ only one is possible)

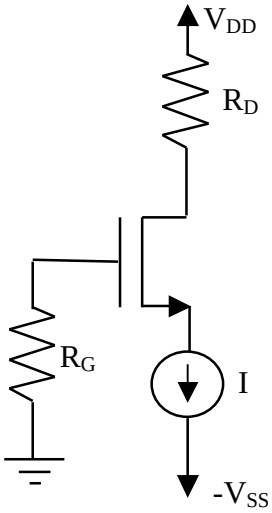
Ex: V_{DD} **= 10 V** R_1 **= 150 kΩ** R_2 **= 100 kΩ** R_S **= 10 kΩ**
R_D **= 50 kΩ** $k'_n(W/L)$ **= 50 μA/V²** V_t **= 1 V**

Solution: I_D **= 100 μA** V_{DS} **= 4 V**

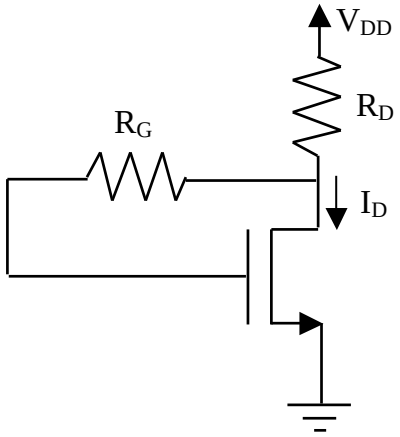
Bias Circuits 2



Two power supplies are available



A simple circuit utilizing a current source



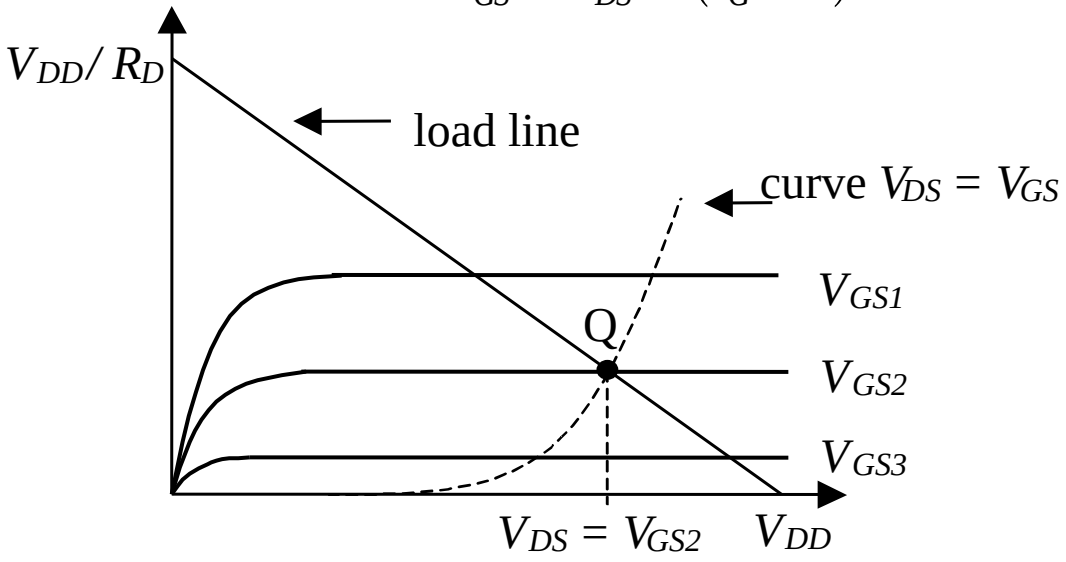
Analysis

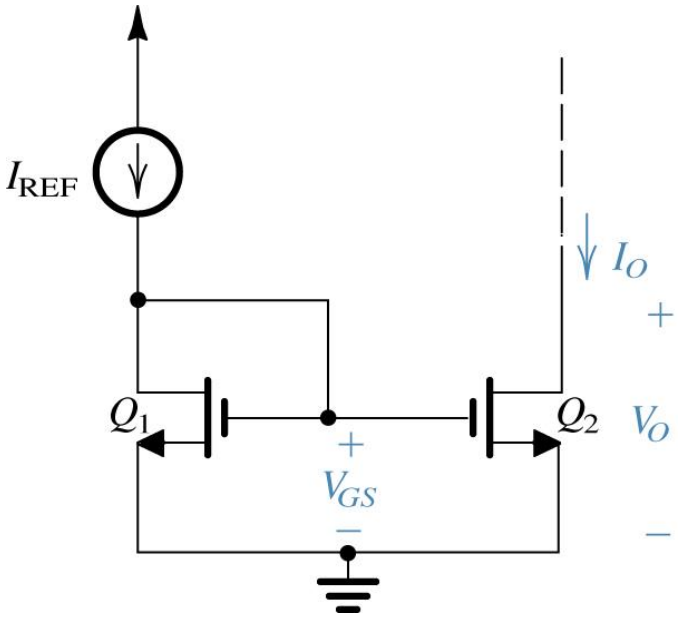
$$I_D = \frac{k_n'}{2} W/L \left(V_{GS} - V_t\right)^2$$

$$V_{GS} = V_{DD} - R_D I_D$$

$$I_D = \frac{k_n'}{2} \left(V_{DD} - V_t - R_D I_D\right)^2$$

$$V_{GS} = V_{DS} \therefore \left(I_G = 0\right)$$





Q_1: $I \rightarrow V$ converter

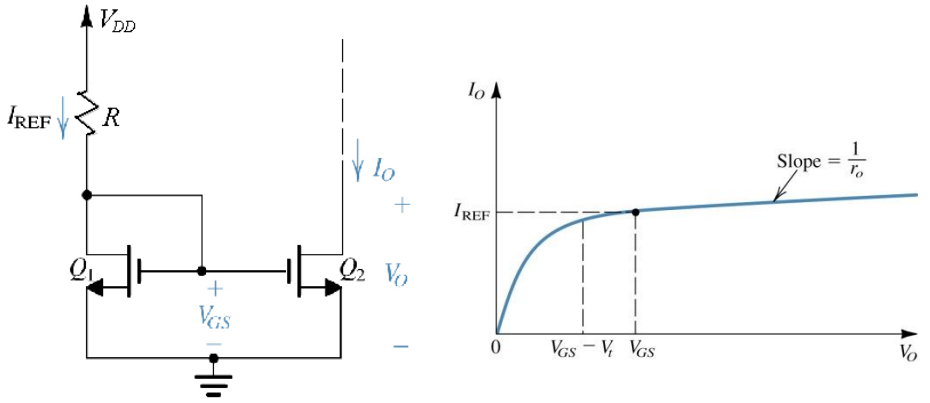
Q_2: $V \rightarrow I$ converter

If Q_2 in saturation

$$\left(v_{o_{\min}} = V_{GS} - V_t\right)$$

then

$$I_o / I_{REF} = \left(W/L\right)_2 / \left(W/L\right)_1$$



Example: V_{DD} = 5V ;I_{REF}=10μA; Q_1 and Q_2 are matched ; L=10 μm *and* W=100 μm; V_t = 1V ; k'_n=20 μ A/V² V_A = 10L; ΔVo=+3V

$$I_{D1} = I_{REF} = 100 = \frac{1}{2} 20 \frac{100}{10} (V_{GS} - 1)^2$$

$$V_{GS} = 2\text{V}$$

$$R = \frac{5-2}{100\mu} = 30K\Omega$$

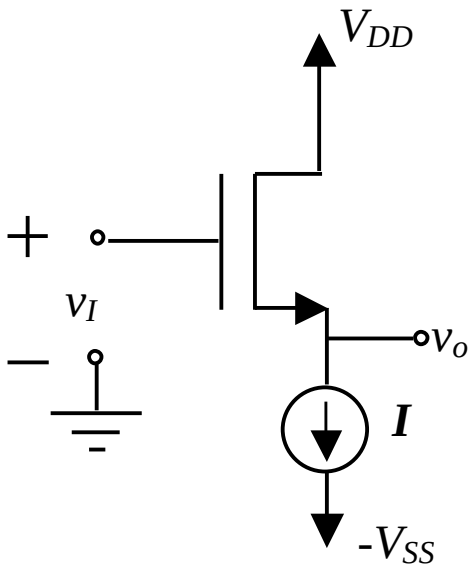
$$v_{o_{\min}} = 2 - 1 = 1\text{V}$$

$$V_A = 10 \text{ x } 10 = 100\text{V} \rightarrow r_o = \frac{100\text{V}}{100\mu A} = 1\text{M}\Omega$$

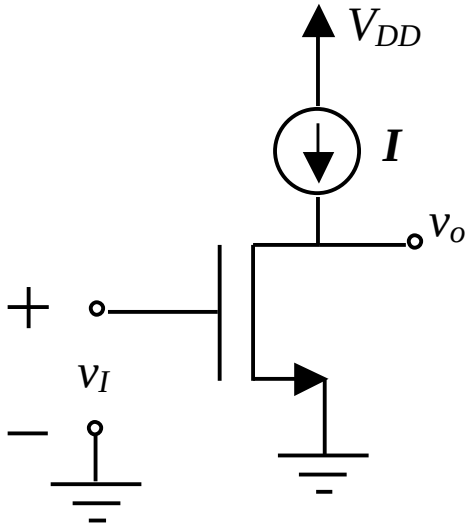
$$\Delta I_o = \frac{\Delta V_o}{r_o} = \frac{3\text{V}}{1\text{M}\Omega} = +3\,\mu\text{A} \Rightarrow +3\%$$

Basic MOSFET current mirror.

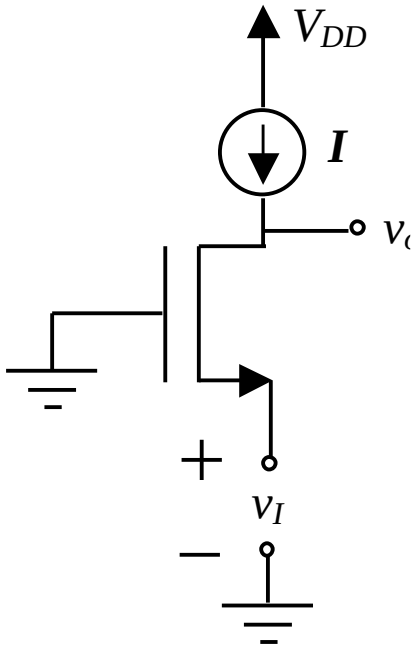
Basic amplifier configurations with current sources



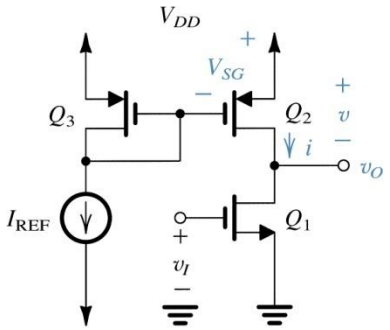
Source follower
or common-drain
amplifier



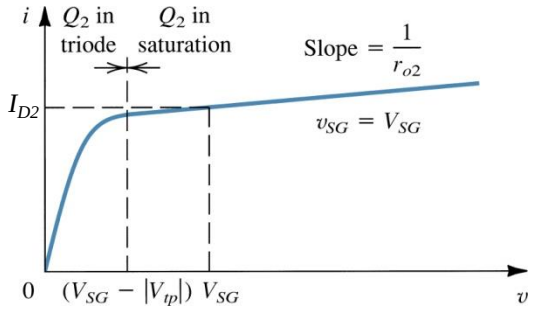
Common-source
amplifier

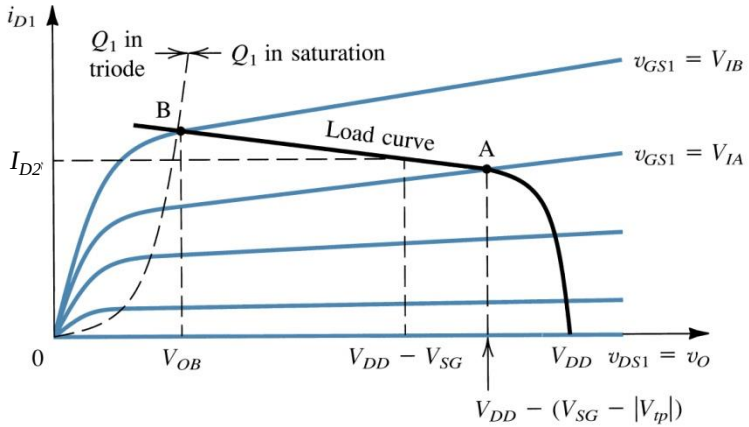


Common-gate
amplifier

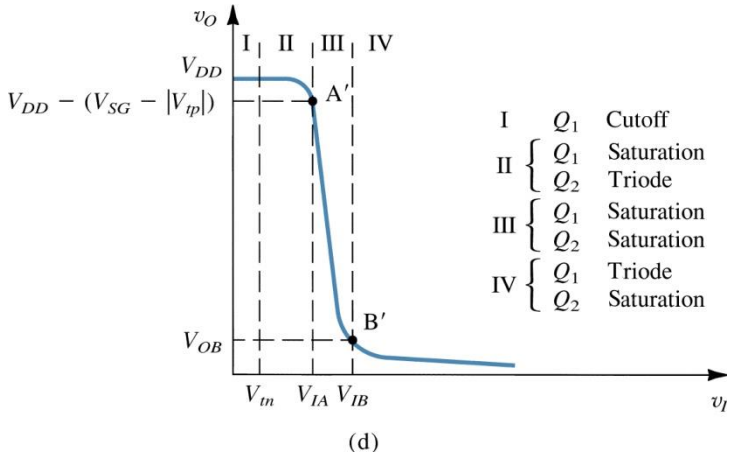


(a)

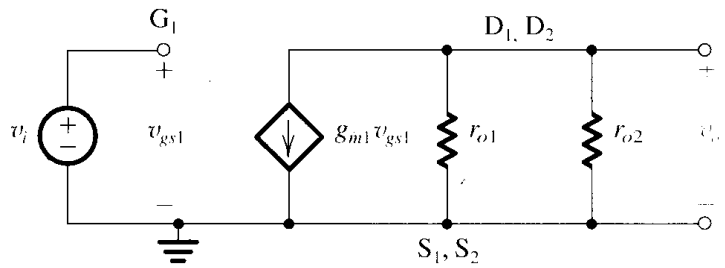




(c)



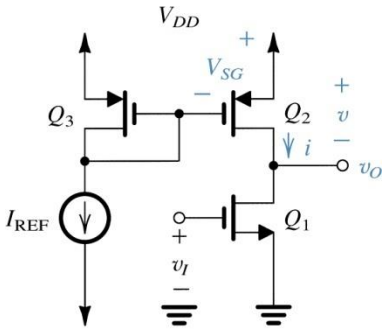
(d)



$$R_i = \infty \quad R_o = r_{o1} // r_{o2}$$

$$A_v = -g_{m1}\left(r_{o1} // r_{o2}\right)$$

The CMOS common-source amplifier: **(a)** circuit; **(b)** *i-v* characteristic of the active-load Q_2; **(c)** graphical construction to determine the transfer characteristic; and transfer characteristic.



(a)

Example: V_{DD}=10V;V_{tn} = | V_{tp}| = 1V ; k'_n= 2 k'_p= 20 μA/V^2
(W=100 μm; L =10 μm |V_A|= 100V for both the n and p device)
I_{REF}=100 μA.

$$I_{REF} = I_{D2} = I_{D1} = 100\,\mu\text{A}$$

$$I_{D3} = I_{REF} = 100\,\mu\text{A} = \frac{1}{2}k'_p\left(\frac{W}{L}\right)_3\left(V_{SG} - |V_{tp}|\right)^2 \Rightarrow V_{SG} = 2.41\text{V}$$

$$v_{O_{\max}} = 10 - (V_{SG} - |V_{tp}|) = 8.59\text{V}$$

$$v_{O_{\min}} \approx V_I - V_{tn} = 1\text{V}$$

$$V_O \approx \left(v_{O_{\max}} - v_{O_{\min}}\right)\frac{r_{o1}}{r_{o1} + r_{o2}} + v_{O_{\min}} = 4.795\text{V}$$

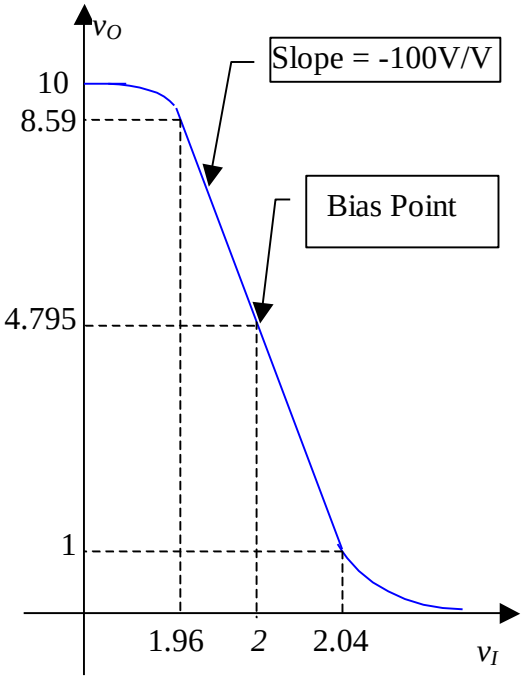
$$I_{D1} = I_{REF} = 100\,\mu\text{A} = \frac{1}{2}k'_n\left(\frac{W}{L}\right)_1\left(V_I - V_{tn}\right)^2 \Rightarrow V_I = 2\text{V}$$

$$g_{m1} = \sqrt{2k'_n\left(\frac{W}{L}\right)_1 I_{REF}} = 0.2m\,\text{A/V}$$

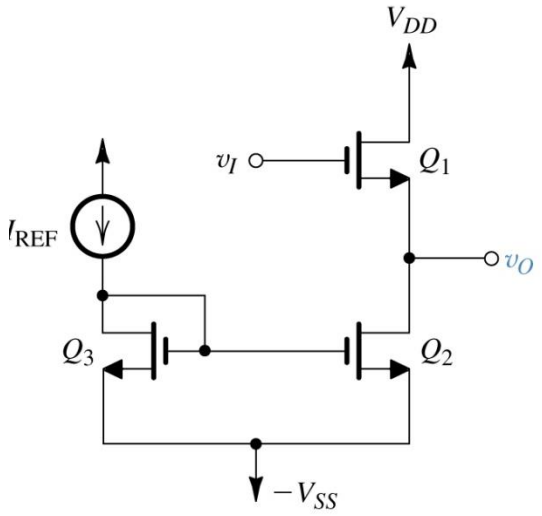
$$r_{o1} = r_{o2} = \frac{|V_A|}{I_{REF}} = 1\text{M}\Omega$$

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{o1} /\!/ r_{o2}\right) = -100\,\text{V/V}$$

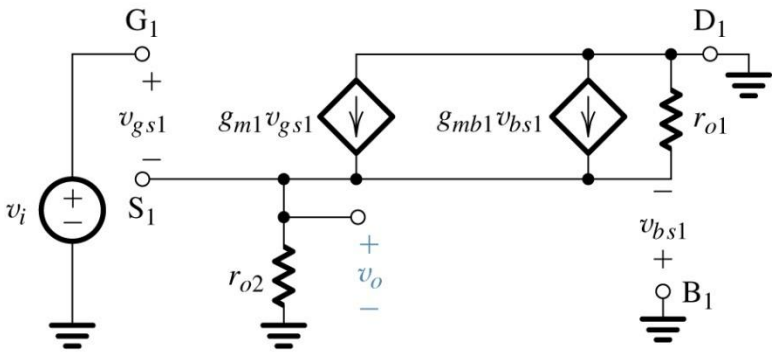
$$R_{in} = \infty \quad \therefore \quad R_o = \left(r_{o1} /\!/ r_{o2}\right) = 0.5\text{M}\Omega$$



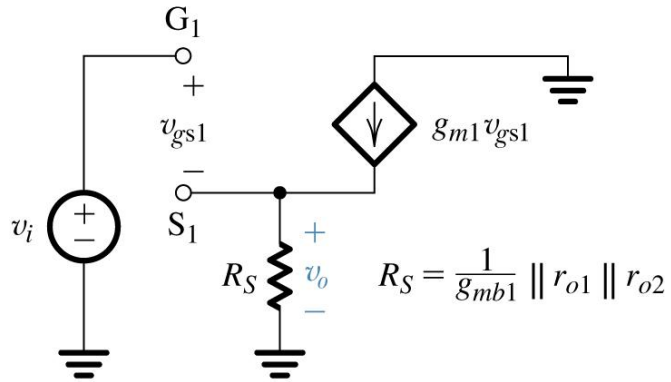
$$\left|\hat{v}_o\right| = \pm 3.795\text{V}_\text{p} \Rightarrow \left|\hat{v}_i\right| = \pm 40\text{mV}_\text{p}$$



(a)



(b)



(c)

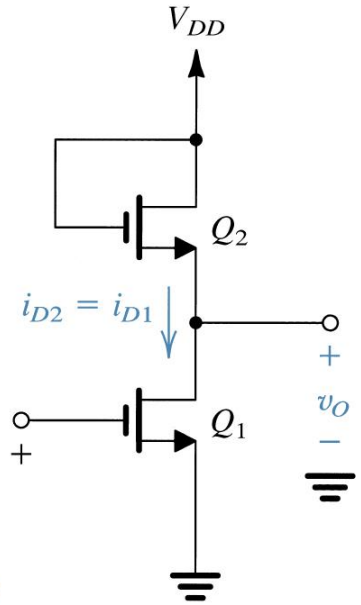
$$A_v \equiv \frac{v_o}{v_i} = \frac{g_{m1}R_S}{1+g_{m1}R_S} = \frac{g_{m1}}{g_{m1}+g_{mb1}+\frac{1}{r_{o1}}+\frac{1}{r_{o2}}}$$

$$A_v \cong \frac{g_{m1}}{g_{m1}+g_{mb1}} = \frac{1}{1+\chi}$$

$$R_o = \left(1/g_{m1}\right) // \left(1/g_{mb1}\right) // r_{o1} // r_{o2}$$

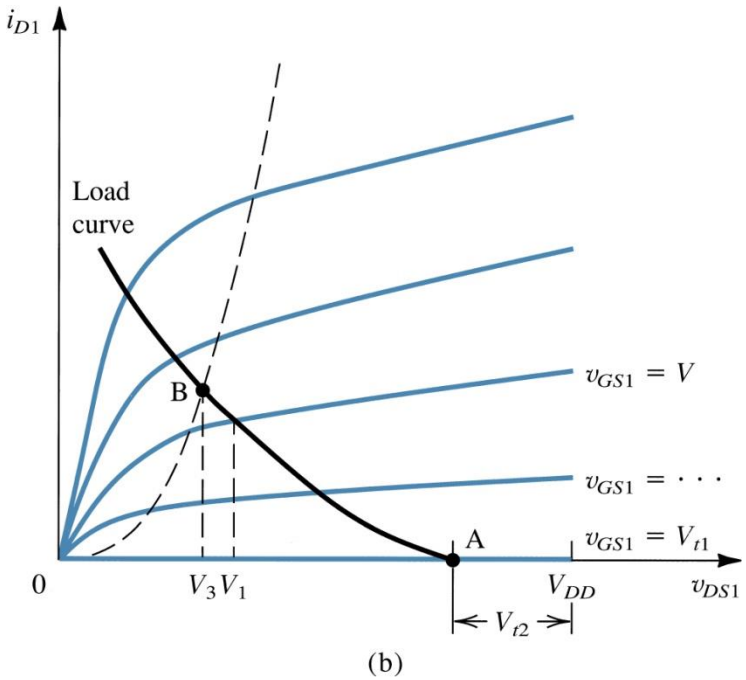
$$R_o \cong \left(1/g_{m1}\right) // \left(1/g_{mb1}\right) = \frac{1}{g_{m1}(1+\chi)}$$

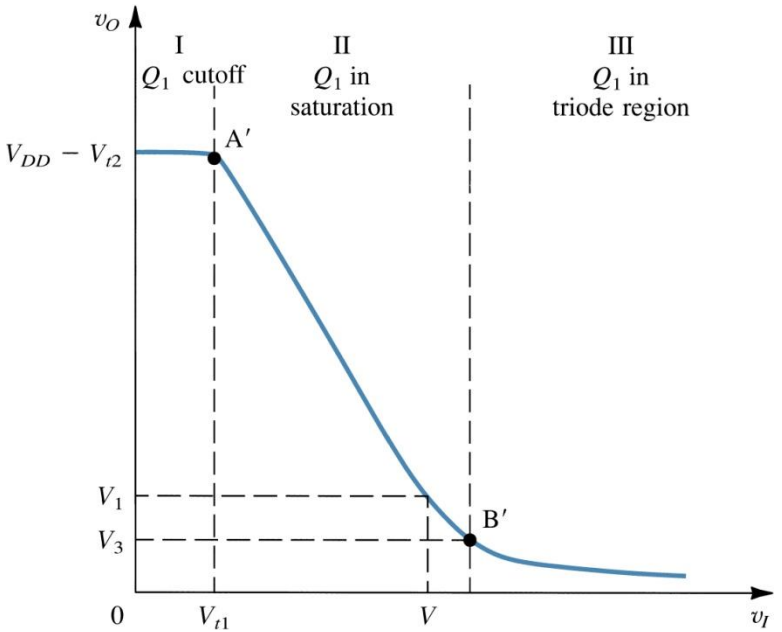
The source follower: **(a)** circuit; **(b)** small-signal equivalent circuit; and **(c)** simplified version of the equivalent circuit.



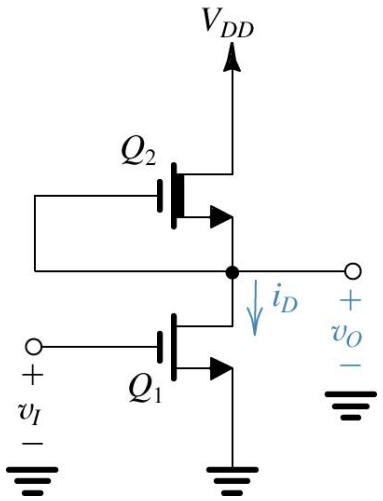
$$v_O = \left(V_{DD} - V_t + \sqrt{\frac{(W/L)_1}{(W/L)_2}} V_t \right) - \sqrt{\frac{(W/L)_1}{(W/L)_2}} v_I$$

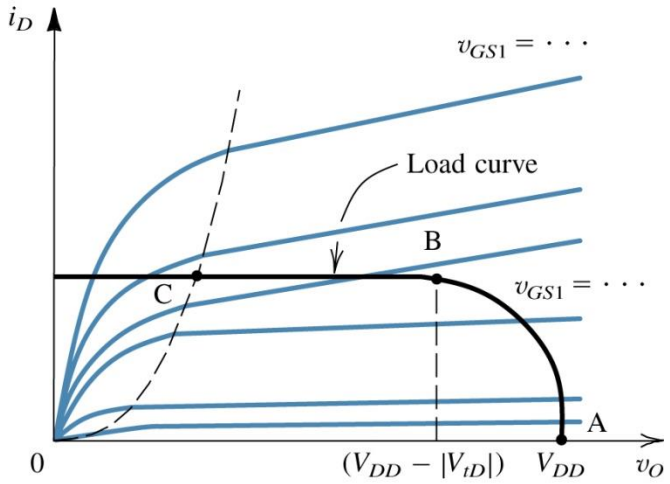
$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1+\chi_2} \cong -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

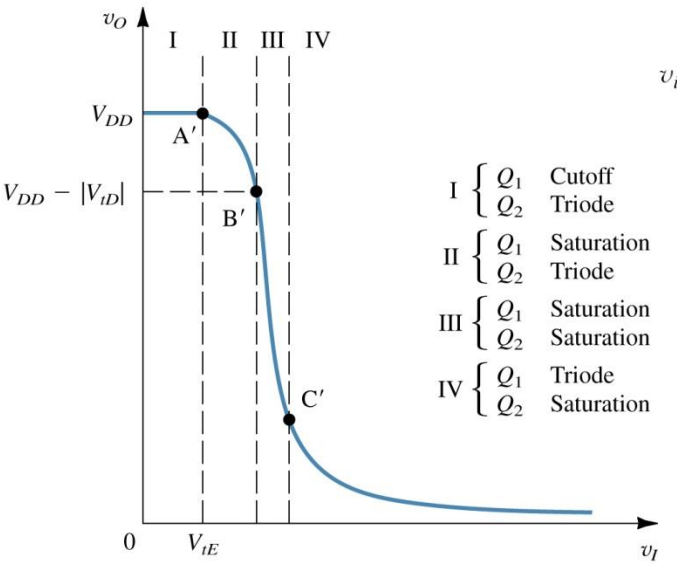


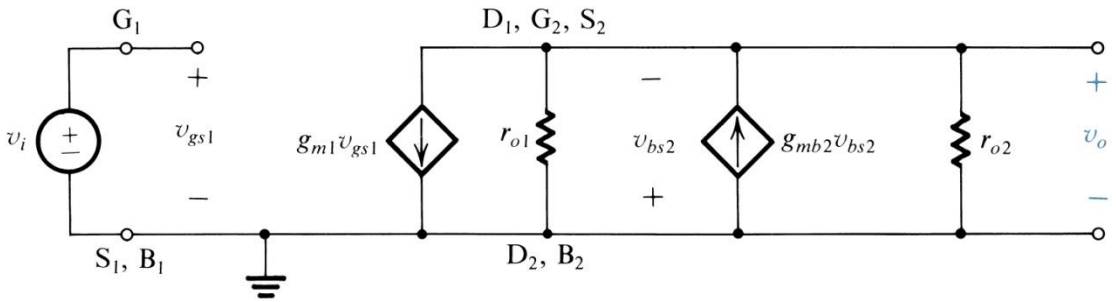


(a) NMOS amplifier with enhancement load; **(b)** graphical determination of the transfer characteristic; **(c)** transfer characteristic.





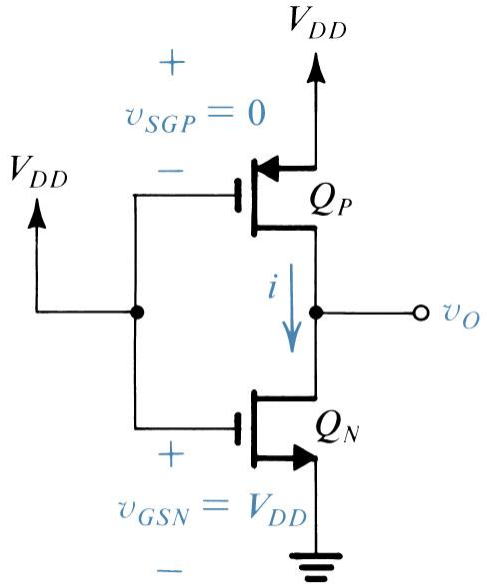




$$A_v \equiv \frac{v_o}{v_i} = -g_{m1}\left[\left(\frac{1}{g_{mb1}}\right) // r_{o1} // r_{o2}\right]$$

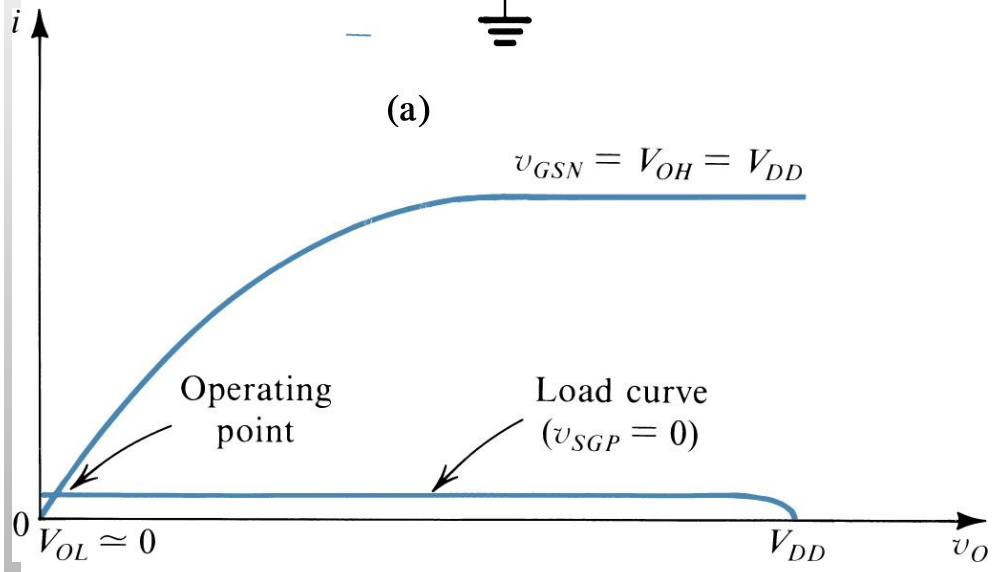
$$A_v \cong -\frac{g_{m1}}{g_{mb2}} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}\,\frac{1}{\chi}$$

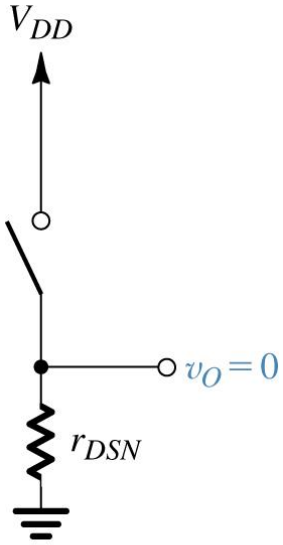
The NMOS amplifier with depletion load: **(a)** circuit; **(b)** graphical construction to determine the transfer characteristic; and **(c)** transfer characteristic.



(a)

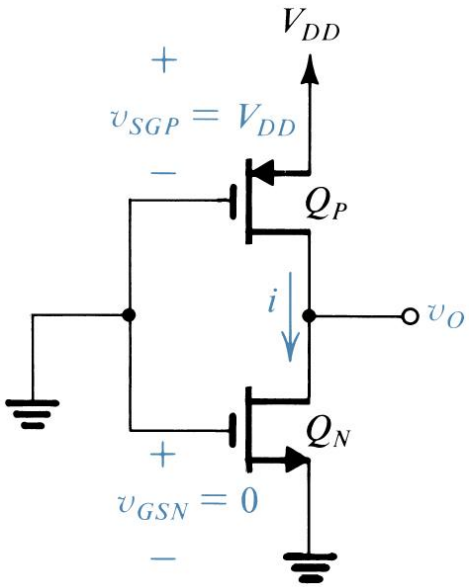
$$r_{DSN} = \frac{1}{\left[k_n'\left(\frac{W}{L}\right)_n\left(V_{DD} - V_{tn}\right)\right]}$$



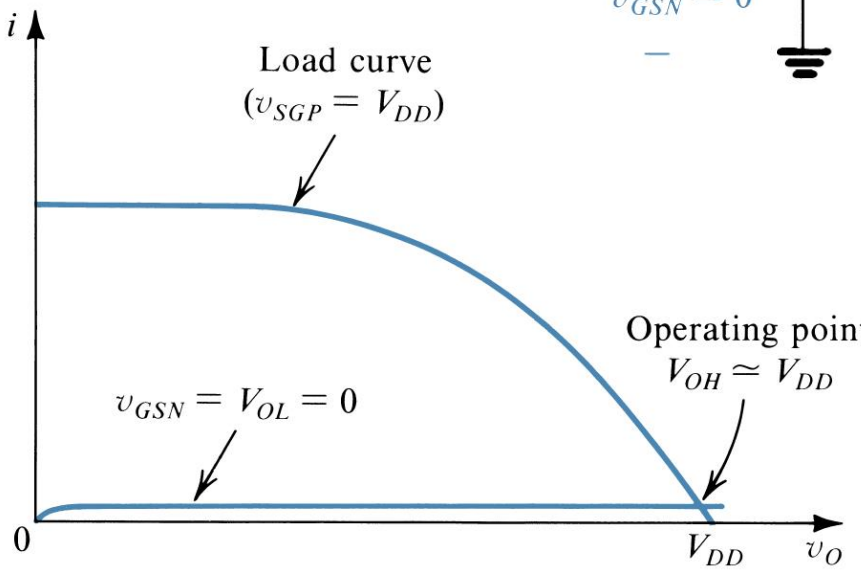


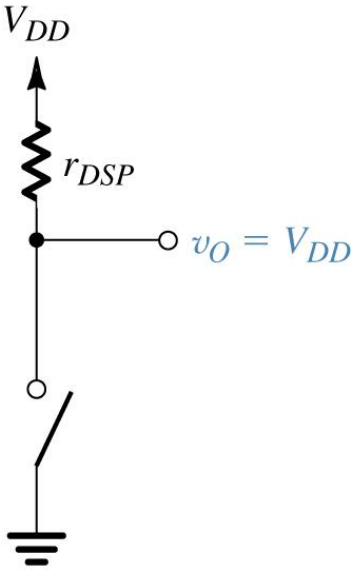
(c)

Operation of the CMOS inverter when v_1 is high: (a) circuit with $v_1 = V_{DD}$ (logic-1 level, or V_{OH}); (b) graphical construction to determine the operating point; and (c) equivalent circuit.



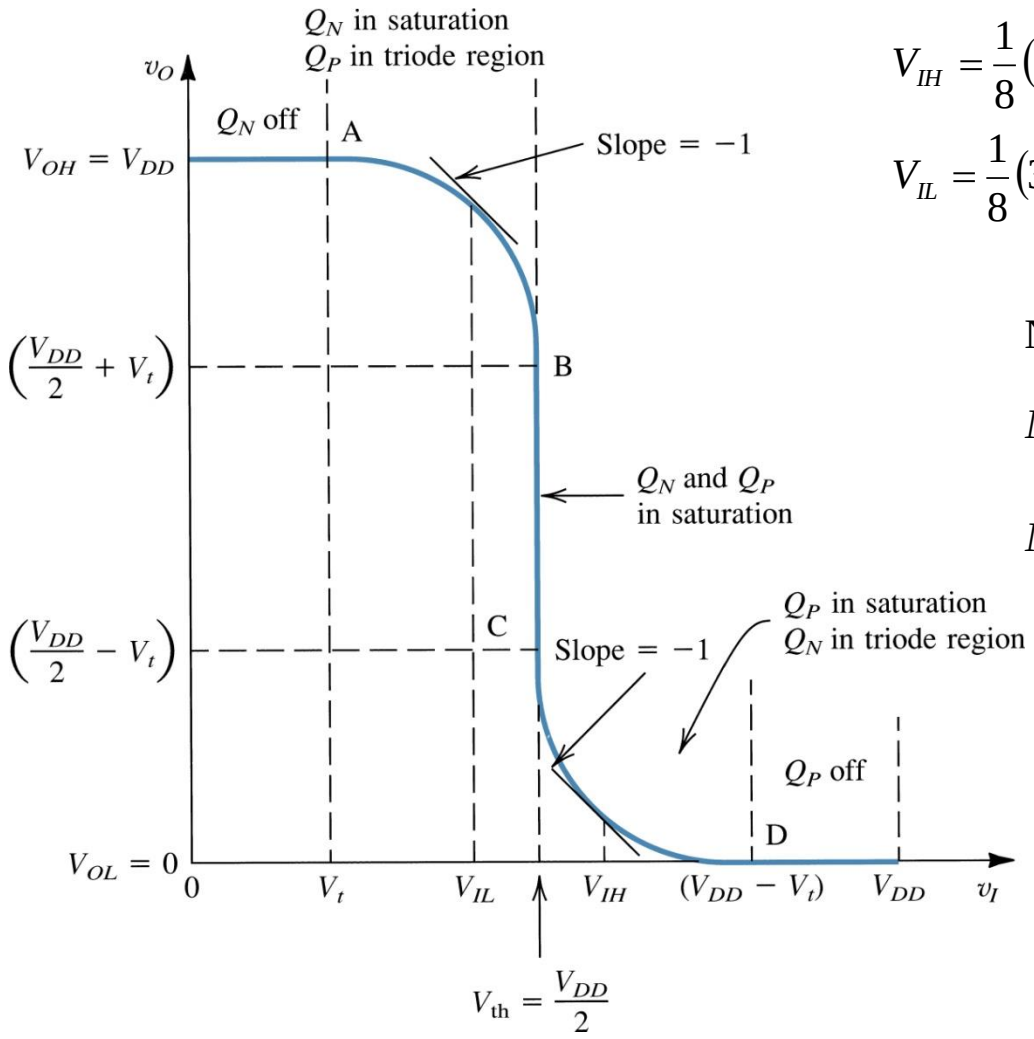
$$r_{DSP} = \frac{1}{\left[k_p'\left(\frac{W}{L}\right)_p\left(V_{DD} - |V_{tp}|\right)\right]}$$





(c)

Operation of the CMOS inverter when v_1 is low: (a) circuit with v_1 = 0V (logic-0 level, or V_{OL}); (b) graphical construction to determine the operating point; and (c) equivalent circuit.



$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

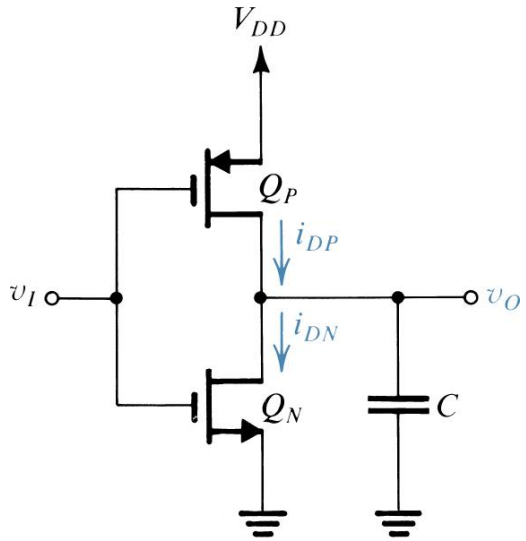
$$V_{IL} = \frac{1}{8}(3V_{DD} - 2V_t)$$

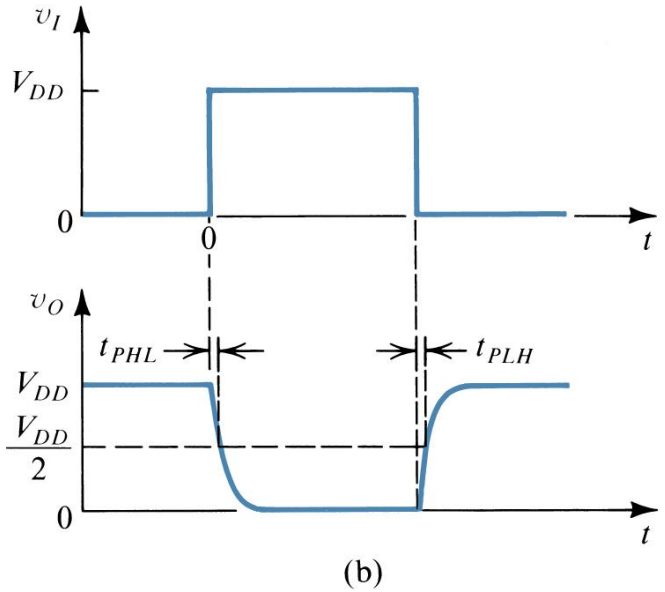
Noise Margins

$$NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$$

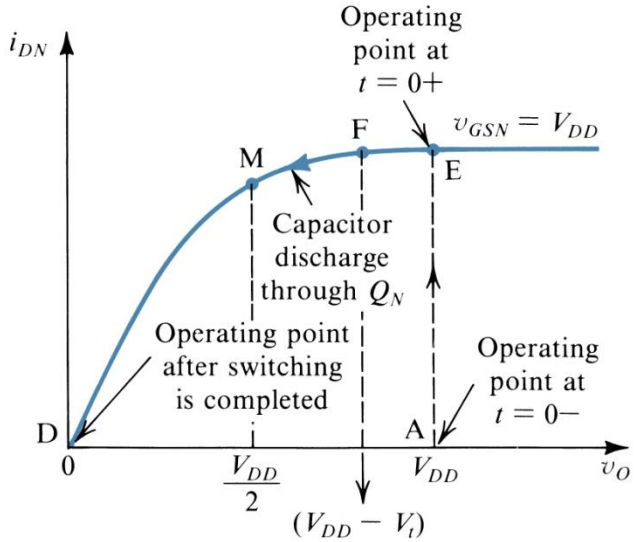
$$NM_L = \frac{1}{8}(3V_{DD} + 2V_t)$$

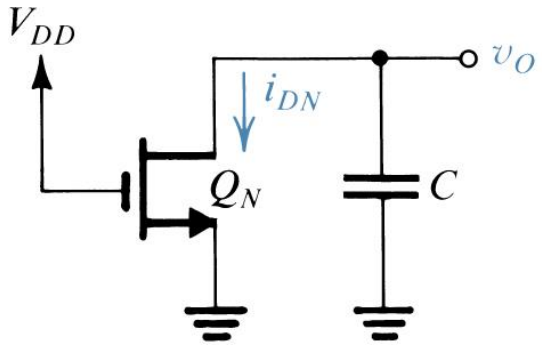
The voltage transfer characteristic of the CMOS inverter.





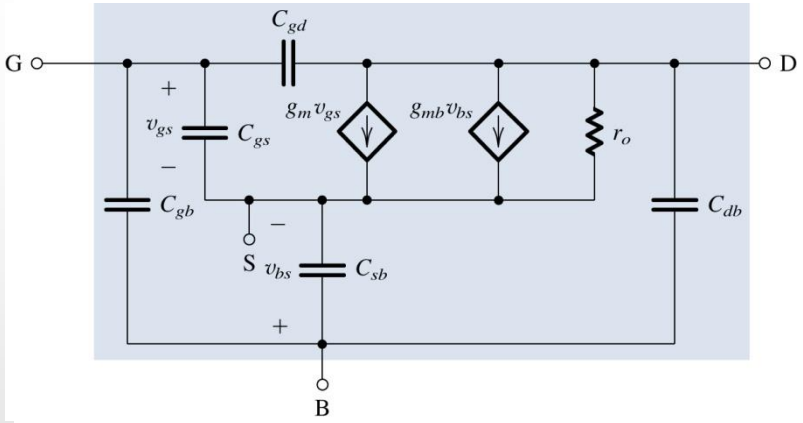
(b)

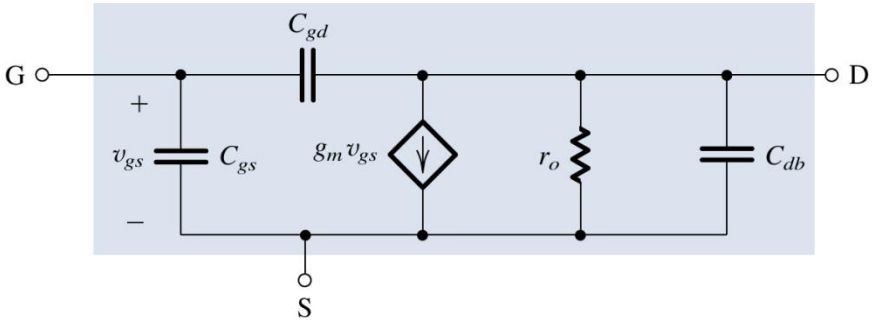




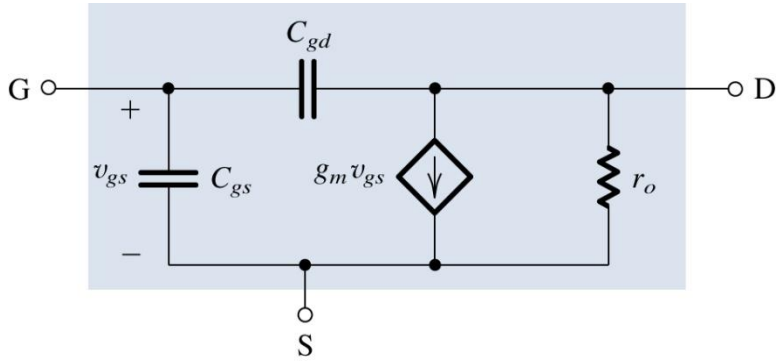
(d)

Dynamic operation of a capacitively loaded CMOS inverter: (a) circuit; (b) input and output waveforms; (c) trajectory of the operating point as the input goes high and C discharges through the Q_N; (d) equivalent circuit during the capacitor discharge.





(b)



(c)

Strong inversion and saturation:

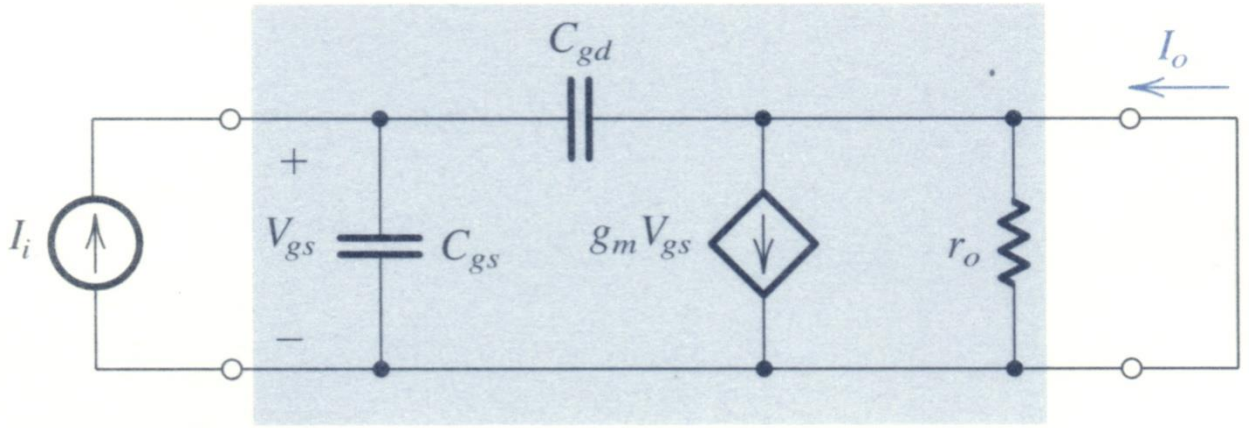
$$V_{GS} - V_t > 200 \text{ mV}$$

$$g_m = \sqrt{2\,k\,(W/L)I_D}$$

$$r_o = \frac{V_A + V_{DS}}{I_D}$$

$$C_{gs} = \frac{2}{3} C_{ox} W L$$

(a) High-frequency equivalent circuit model for the MOSFET; (b) the equivalent circuit for the case the source is connected to the substrate (body); (c) the equivalent circuit model of (b) with C_{db} neglected (to simplify analysis).



$$\frac{I_o}{I_i} = \frac{g_m}{s\left(C_{gs} + C_{gd}\right)}$$

For physical frequencies $s = j\omega$, it cam be seen that the magnitude of the current gain becomes unity at the frequency:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}$$

Determining the short-circuit current gain I_o/I_i.

When to use JFETs

- ✓ JFET have much higher input impedances and much lower input currents than BJTs.
- ✓ BJTs are more linear than JFETs.
- ✓ The gain of a BJT is much higher than that of a JFET.

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