Metal-Oxide-Semiconductor Fields Effect Transistors (MOSFETs)

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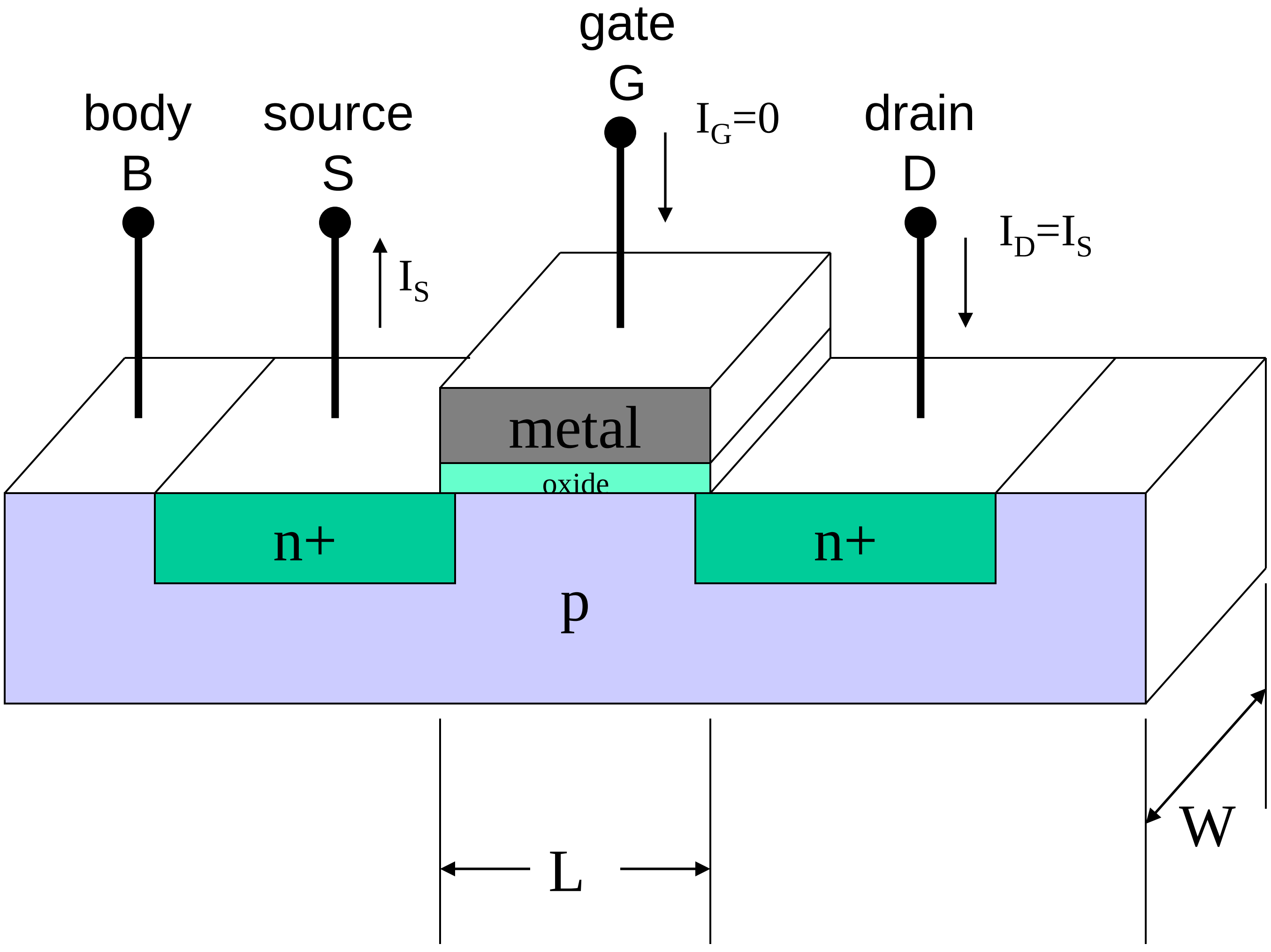
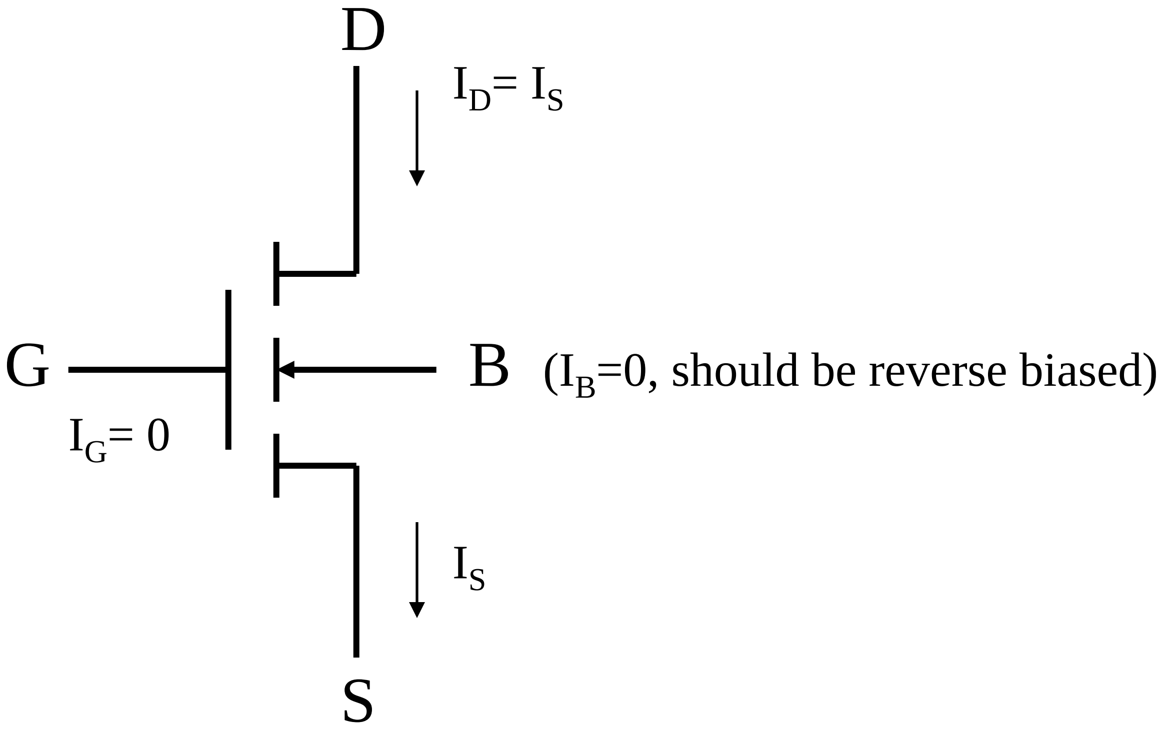
Structure: *n-channel* MOSFET (NMOS)

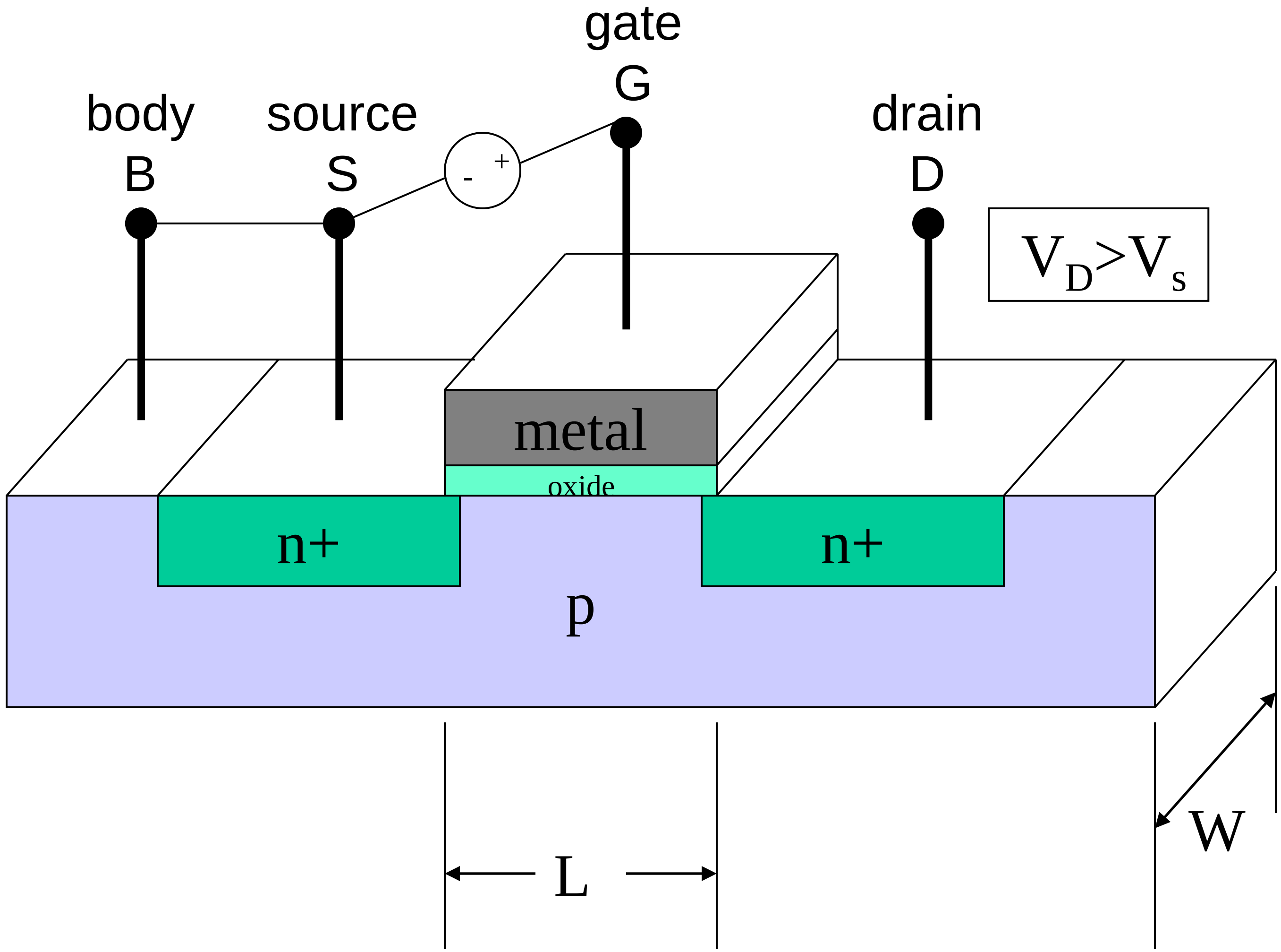


Circuit Symbol (NMOS)



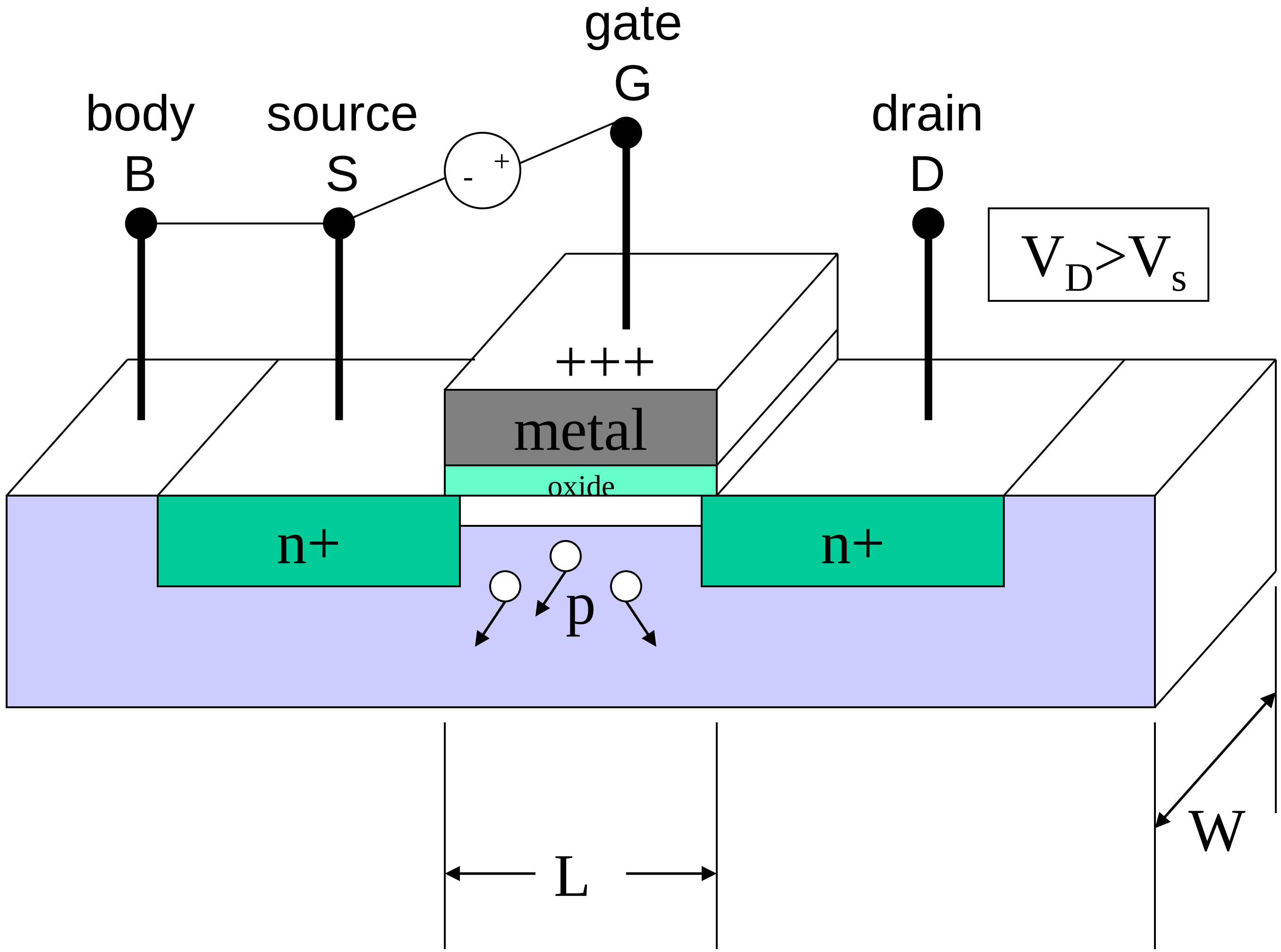
$$V_{GS} = 0$$

n^+pn^+ structure → $I_D = 0$



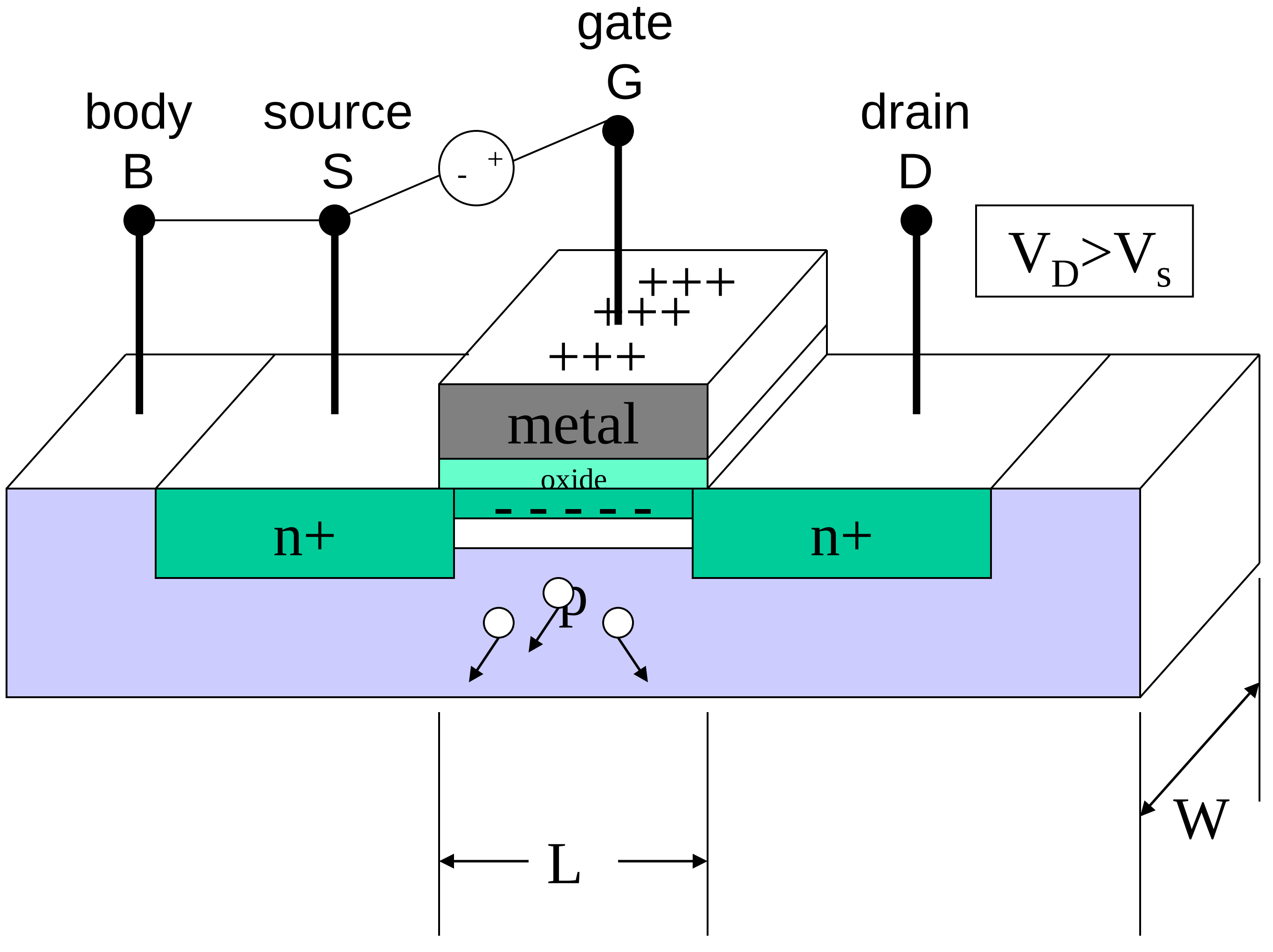
$0 < V_{GS} < V_t$

n^+-depletion-n^+ structure → $I_D = 0$



$V_{GS} > V_t$

n^+-n-n^+ structure → $I_D > 0$

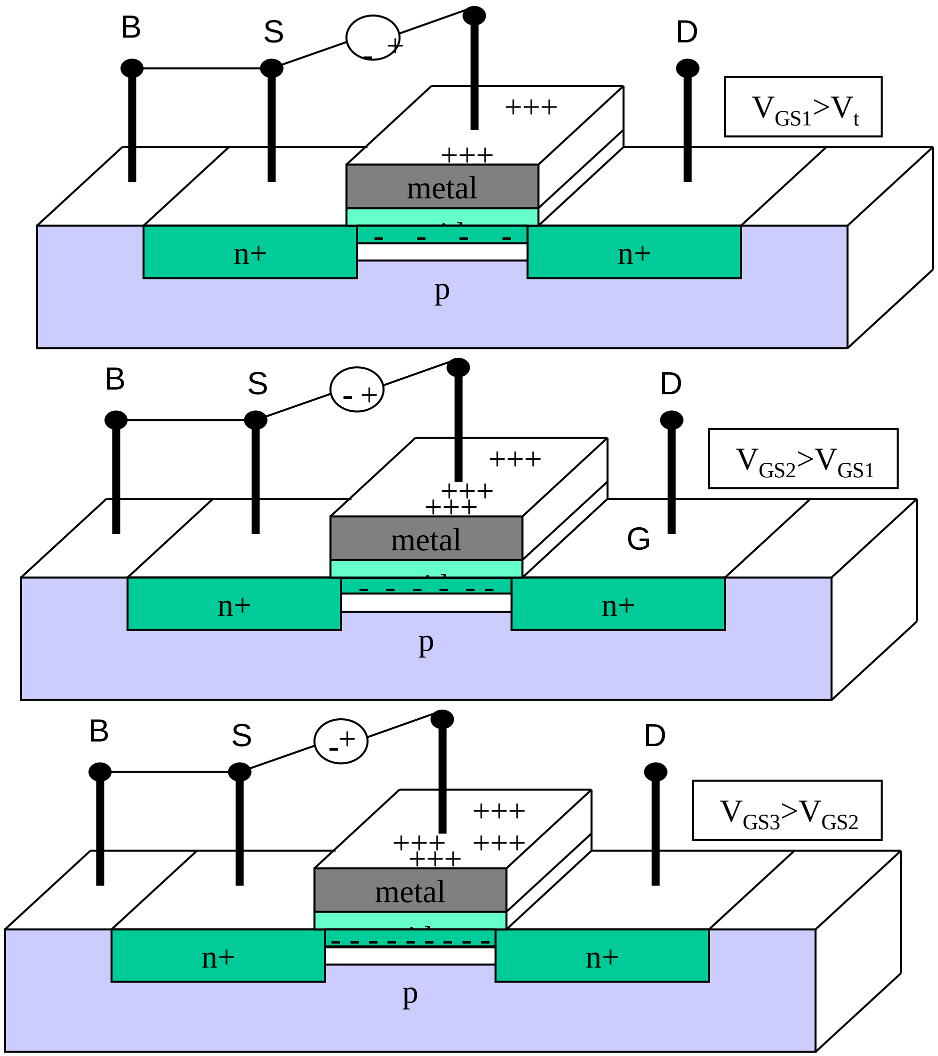


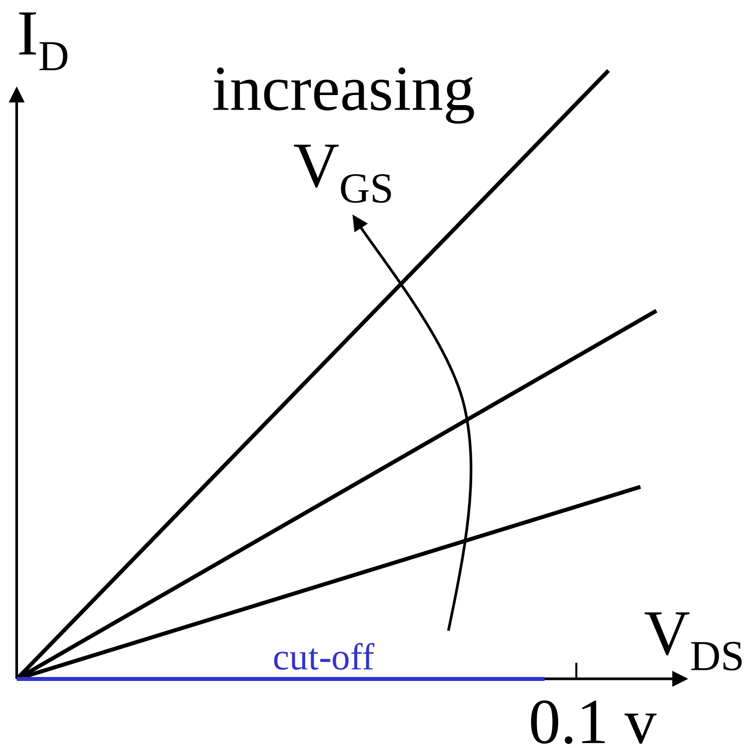
Summary

- V_t is the *threshold voltage*
- If $V_{GS} < V_t$, then there is insufficient positive charge on the gate to *invert* the p-type region
  - This is called “cut-off”
- If $V_{GS} > V_t$, then there is sufficient charge on the gate to attract electrons and invert the p-type region, creating an **n-channel** between the source and drain
  - The MOSFET is now “on”
  - 2 modes of operation: *triode* and *saturation*

Triode Region

A voltage-controlled resistor *@small* V_{DS}



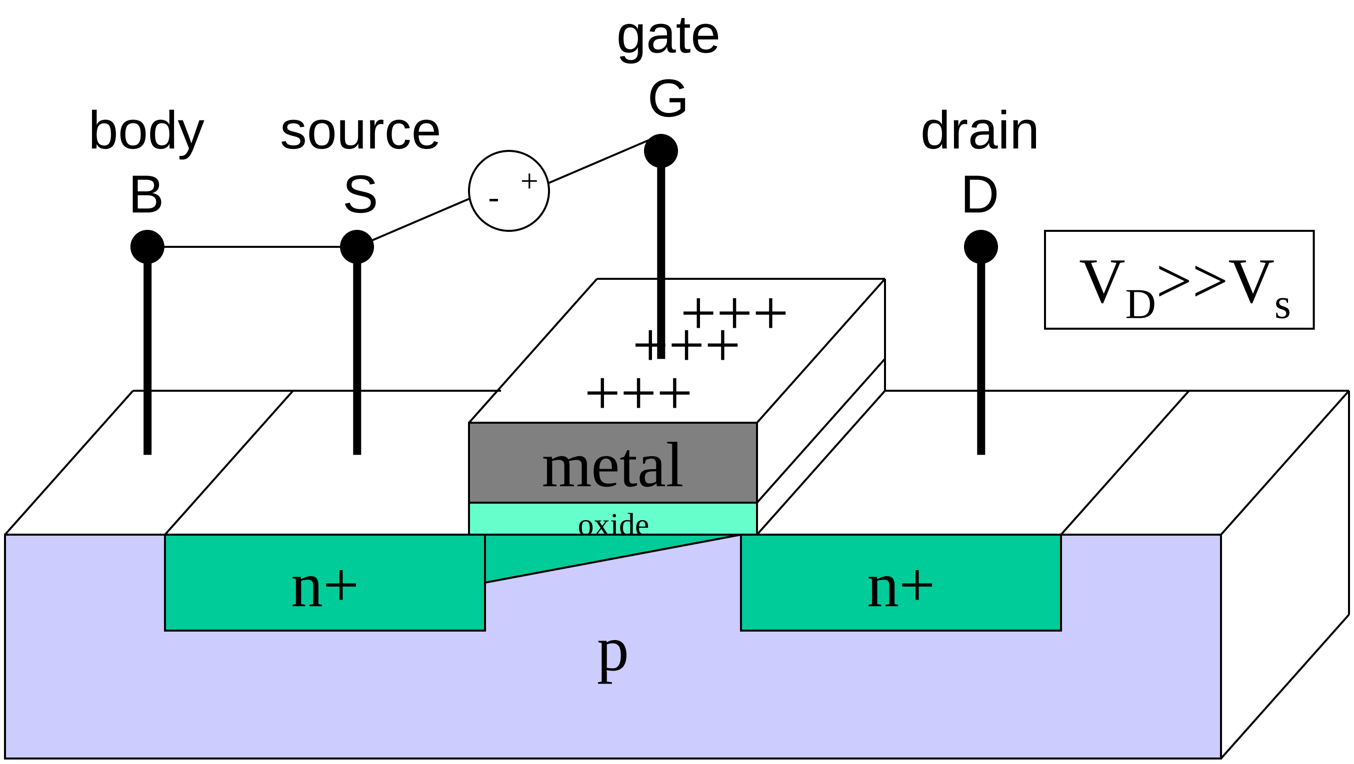


Increasing V_{GS} puts more charge in the channel, allowing more drain current to flow

Saturation Region

occurs at large V_{DS}

As the drain voltage increases, the *difference* in voltage between the drain and the gate becomes *smaller.* At some point, the difference is too small to maintain the channel near the drain → *pinch-off*

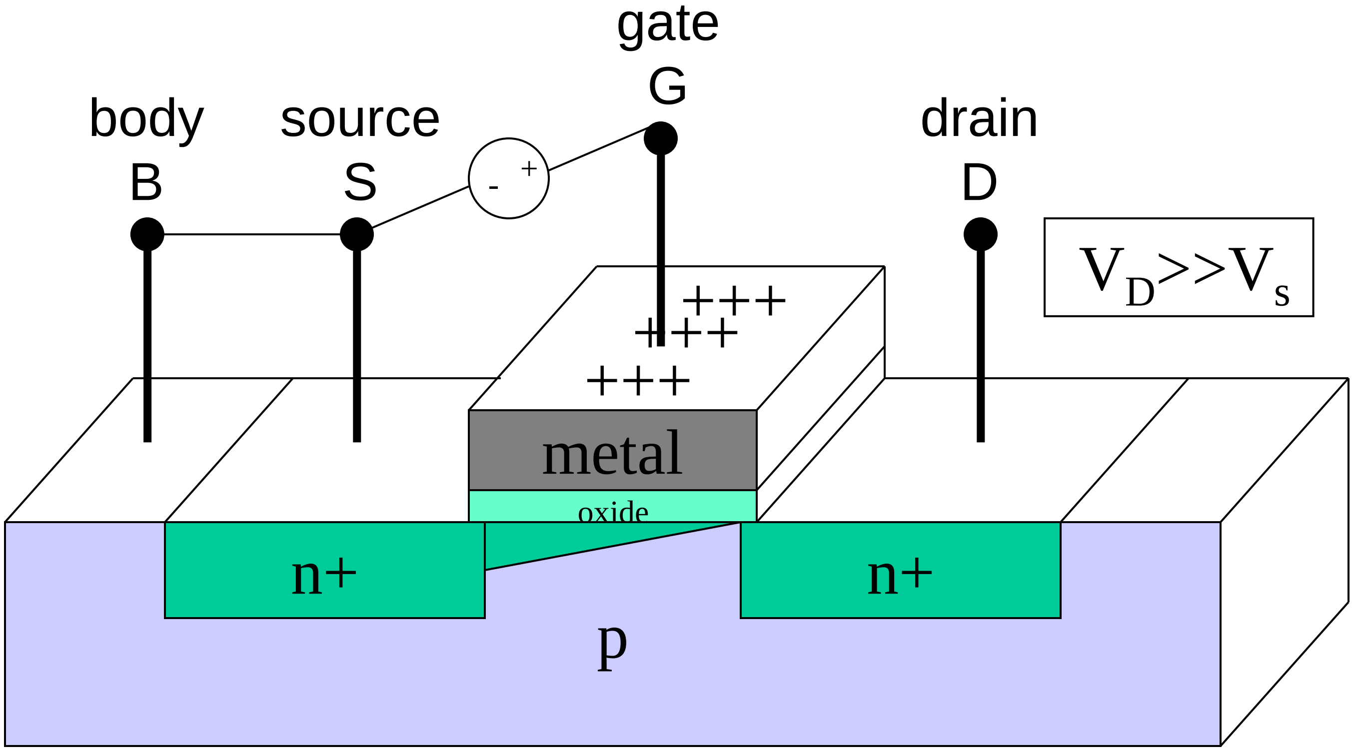


Saturation Region

occurs at large V_{DS}

The *saturation region* is when the MOSFET experiences pinch-off.

Pinch-off occurs when $V_G - V_D$ is less than V_t.



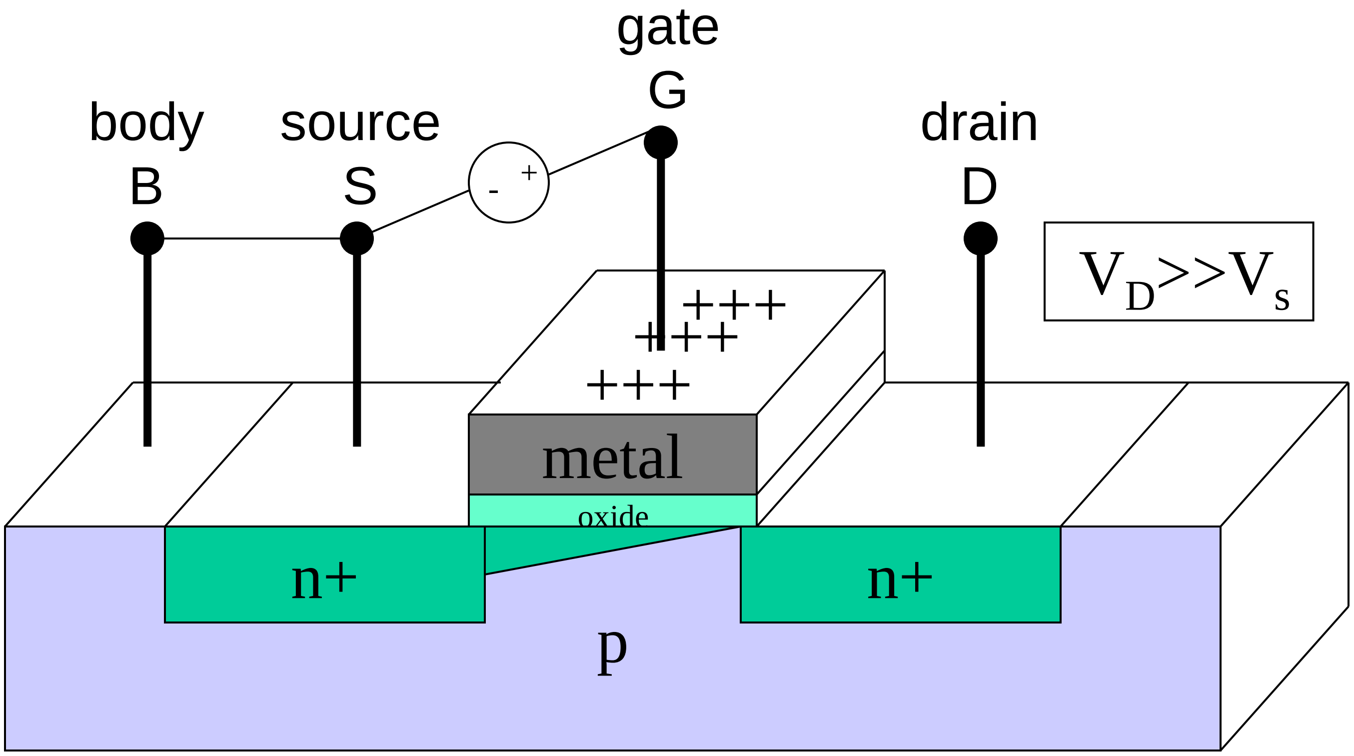
Saturation Region

occurs at large V_{DS}

$V_G - V_D < V_t \ldots$

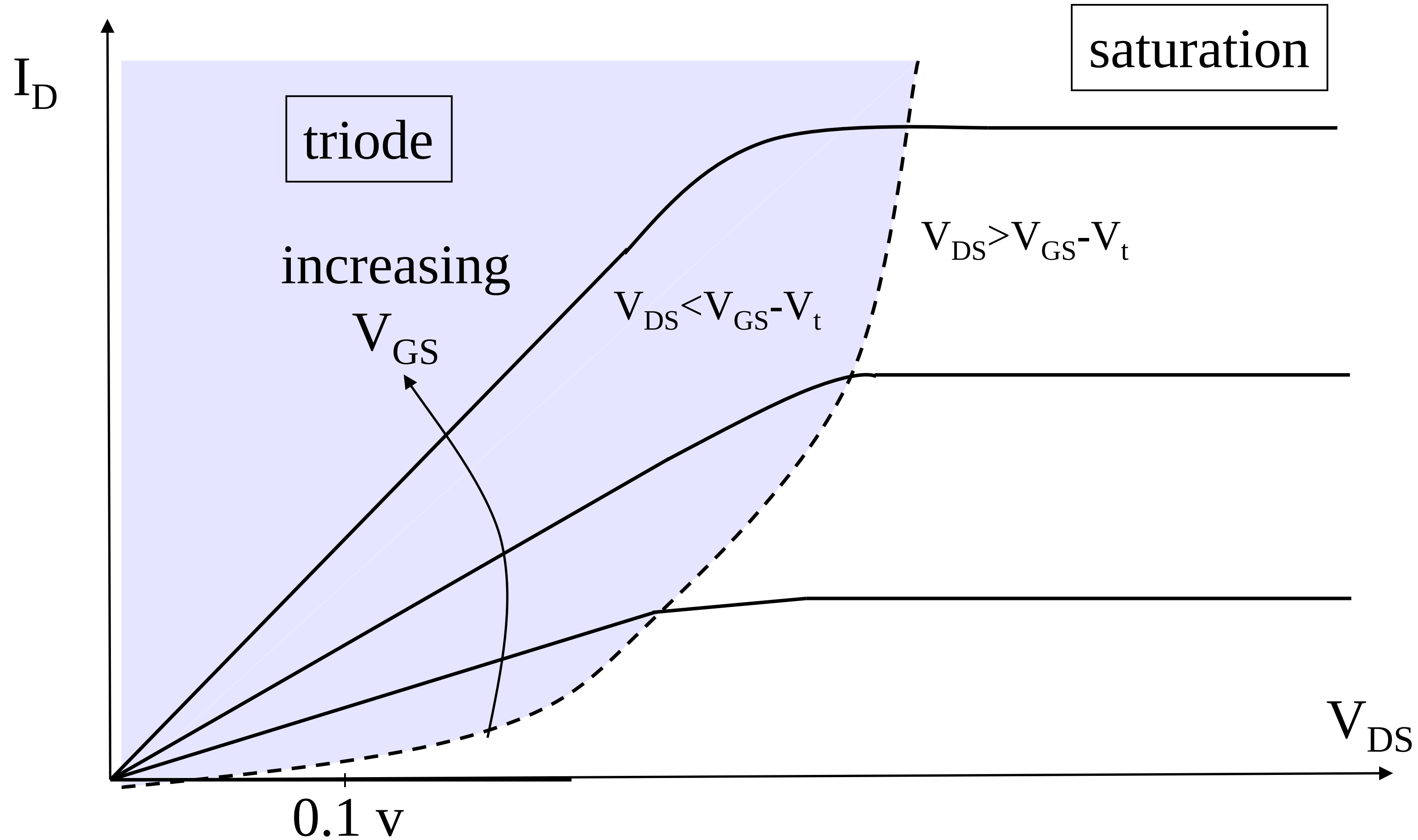
$V_{GS} - V_{DS} < V_t \ldots$

$\mathbf{V_{DS} > V_{GS} - V_t}$



Saturation Region

once pinch-off occurs, there is no further increase in drain current



Simplified MOSFET I-V Equations

Cut-off: $v_{GS} < V_t$

$i_D = i_S = 0$

Triode: $v_{GS} > V_t$ and $v_{DS} < v_{GS} - V_t$

$i_D = k_n'(W/L)[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$

Saturation: $v_{GS} > V_t$ and $v_{DS} > v_{GS} - V_t$

$i_D = \frac{1}{2}k_n'(W/L)(v_{GS} - V_t)^2$

where k_n' = (electron mobility)x(gate capacitance)

$= \mu_n(\varepsilon_{ox}/t_{ox})$ …*electron velocity* = $\mu_n \boldsymbol{E}$

and V_t depends on the doping concentration and gate material used

Electrostatic Discharge (ESD)

- The gate oxide is very thin
  - $t_{ox} < 10$ nm (10×10^{-9} m)
- It is very easy for static electricity to destroy this very thin insulating layer
- Must practice precautions, such as wrist straps and static free work areas

Parasitic Capacitance

- Notice that the entire gate structure looks exactly like a capacitor (metal-insulator-semiconductor)
- This parasitic capacitance at the gate allows current to flow at high frequencies!

  $i_G > 0$ *as frequency increases*

  and, just like other semiconductor devices, the parasitic capacitance limits the speed of the device (turning the MOSFET "on" requires charging the gate capacitance). The $R_{sig}C_{gate}$ *time constant* tells us the signal delay for digital circuits and the upper cut-off frequency for analog circuits.

Conclusion

- For the remainder of the class, we will look at the behavior of semiconductor devices in much more detail

- Occasionally, you might get caught-up in the details! Please refer back to this overview to see how it all fits together.