SUBJECT-BASIC ELECTRONICS ENGINEERING

TOPIC-FIELD EFFECT TRANSISTOR

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Topic includes

- ➢ **Construction and operation of JFET**
- ➢ **Construction and operation of D-MOSFET**
- ➢ **Construction and operation of E-MOSFET**

FIELD EFFECT TRANSISTOR (FET)

There are three types of FETs: JFETs, MOSFETs, and MESFETs. Further, MOSFETs are classified into depletion type and enhancement-type (D-MOSFET and E-MOSFET).

1. JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

The field-effect transistor (FET) is a three-terminal device.The three terminals are gate(G), source (S) and Ddrain (D).The FET is voltage controlled device. Just as there are npn and pnp bipolar transistors, there are n-channel and p-channel field effect transistors.

The term field effect in the name deserves some explanation. For the FET an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

FETs are of three types : the junction field-effect transistor (JFET), the metal–oxide–semiconductor field-effect transistor (MOSFET), and the metal – semiconductor field-effect transistor (MESFET). The MOSFET category is further broken down into depletion and enhancement (i.e. D-MOSFET and E=MOSFET).

Difference between BJT and FET

BJT	FET
Current controlled device	Voltage controlled device
Bipolar (current conduction due to flow of holes and electrons)	Uniploar (current conduction due to flow of majority charge carriers)
Low input impedance as compared to FET	High input impedance
Ac voltage gain is high	Ac voltage gain is low
Less temperature stable	More temperature stable
Larger in size	Smaller in size

Construction and Characteristics of JFET

The basic construction of the n -channel JFET is shown in Fig.1. major part of the structure is the n -type material, which forms the channel between the embedded layers of p -type material. The top of the n -type channel is connected through an ohmic contact to a terminal referred to as the drain (D) , whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). The two p -type materials are connected together and to the gate (G) terminal. In essence, therefore, the drain and the source are connected to the ends of the n -type channel and the gate to the two layers of p -type material.

Operation of JFET

In the absence of any applied potentials the JFET has two $p - n$ junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 1 , that resembles the same region of a diode under no-bias conditions. So, depletion region is void of free carriers and is therefore unable to support conduction.
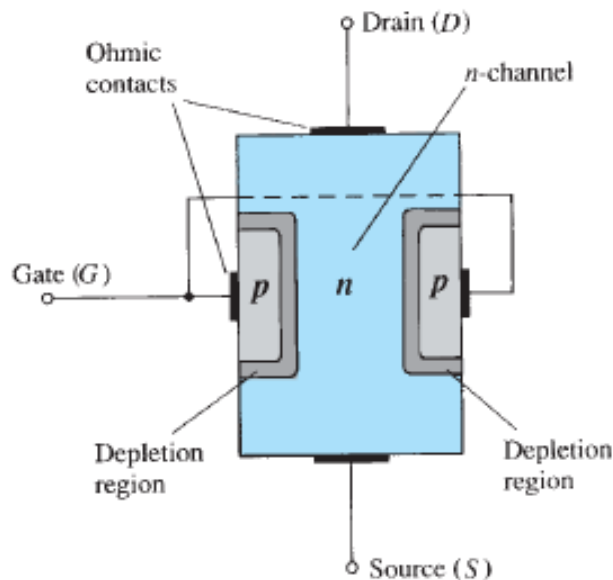

Fig 1. Junction field effect transistor (JFET)

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 2 , a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each p –material similar to the

distribution of the no-bias conditions of Fig. 1 . The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 2 . The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in Fig. 2 , the flow of charge is relatively uninhibited and is limited solely by the resistance of the n -channel between drain and source.

It is seen that the depletion region is wider near the top of both p –type materials. The reason for the change in width of the region is best described through the help of Fig. 3 . Assuming a uniform resistance in the n -channel, we can break down
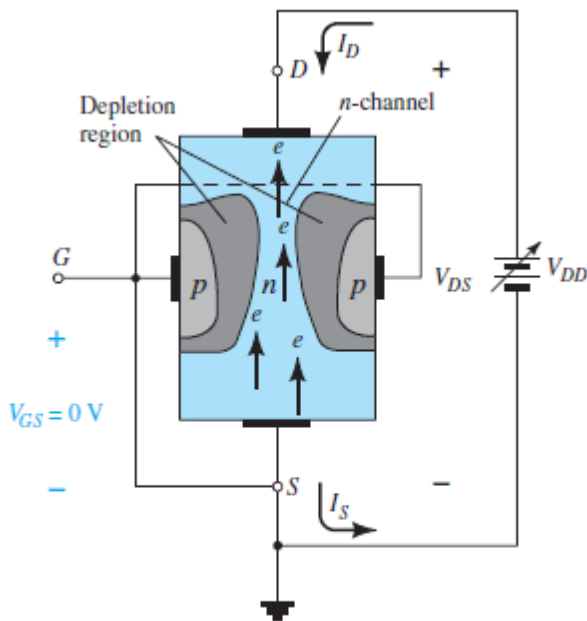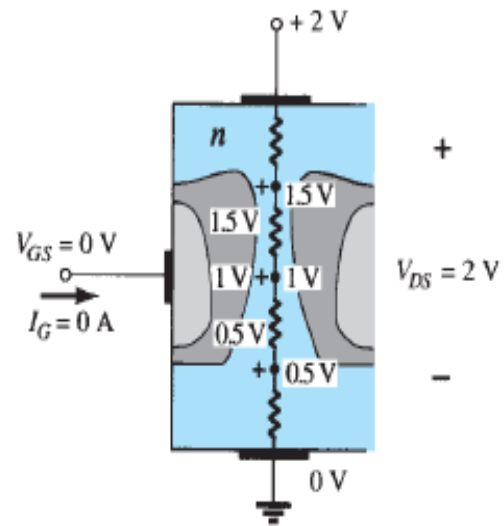
Fig. 2. JFET at V_{GS}=0V and V_{DS}>0V

Fig.3 Varying reverse-bias potential across the

p-n juction of an n-channel JFET

the resistance of the channel into the divisions appearing in Fig. 3 . The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the p -type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. The greater the applied reverse bias, the wider is the depletion region—hence the distribution of the depletion region as shown in Fig. 3 . The fact thatthe p – n junction is reversebiased for the length of the channel results in a gate current of zero amperes, as shown in the same figure.

As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 4 .
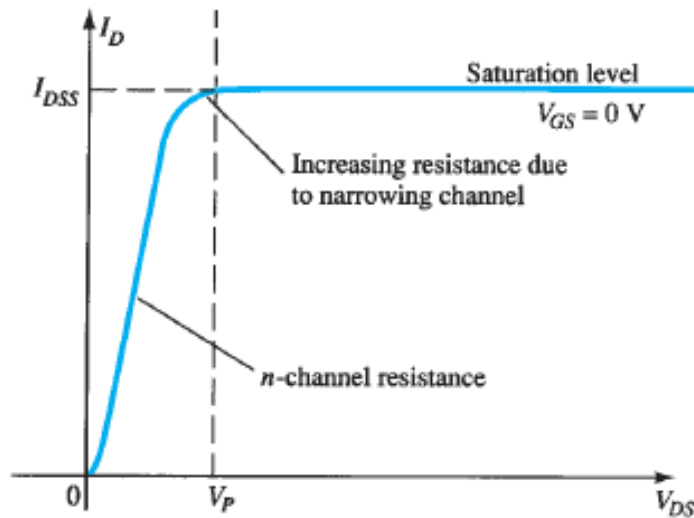
Fig. 4. I_D versus V_{DS} for V_{GS}=0V

The relative straightness of the plot reveals that for the region of low values of V_{DS} , the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 4 , the depletion regions of Fig. 2 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 4 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 5 , a condition referred to as pinch-off will result. The level of V_{DS} that establishes this condition is referred to as the pinch-off voltage and is denoted by V_P , as shown in Fig. 4 .
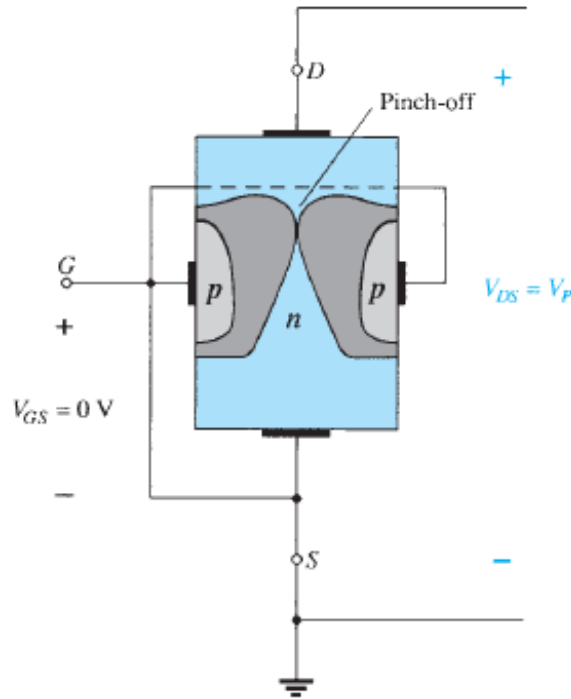
Fig. 5. Pinch-off (V_{GS}=0V, V_{DS}=V_P)

In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig.4, however, this is hardly the case – I_D maintains a saturation level defined as I_{DSS} in Fig. 4 . In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 4 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the n - channel material to establish the varying levels of reverse bias along the $p - n$ junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

As V_{DS} is increased beyond V_P , the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$, the JFET has the characteristics of a current source. As shown in Fig. 6 , the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $>V_P$) is determined by the applied load.
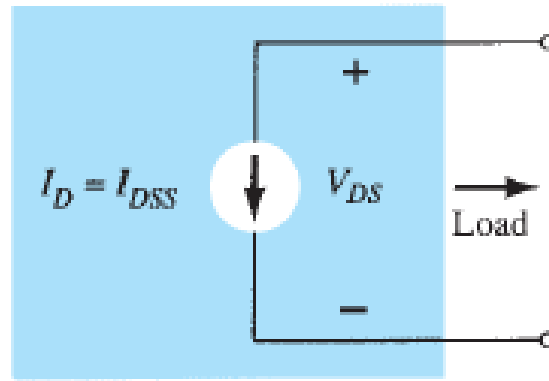
Fig.6 Current source equivalent for $V_{GS}=0V$, $V_{DS}>V_P$.

The choice of notation I_{DSS} is derived from the fact that it is the *d*rain-to- *s*ource current with a *s*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} >|V_P|$.

V GS < 0 V
The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of *V* $_{GS}$ can be developed for the JFET. For the *n* - channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.
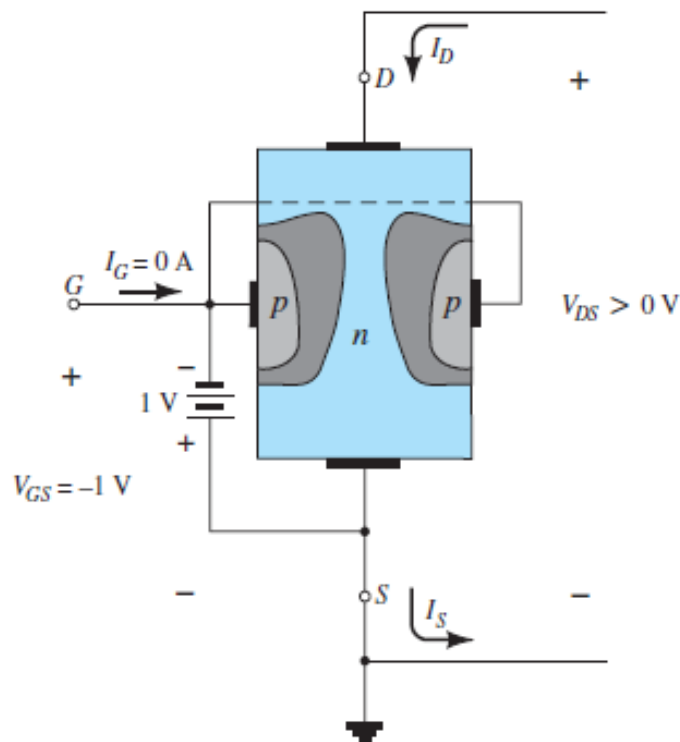
Fig.7. Application of anegative voltage to the gate of a JFET.

In Fig. 7 a negative voltage of -1 V is applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V, but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in Fig. 8 for $V_{GS} = -1$ V.
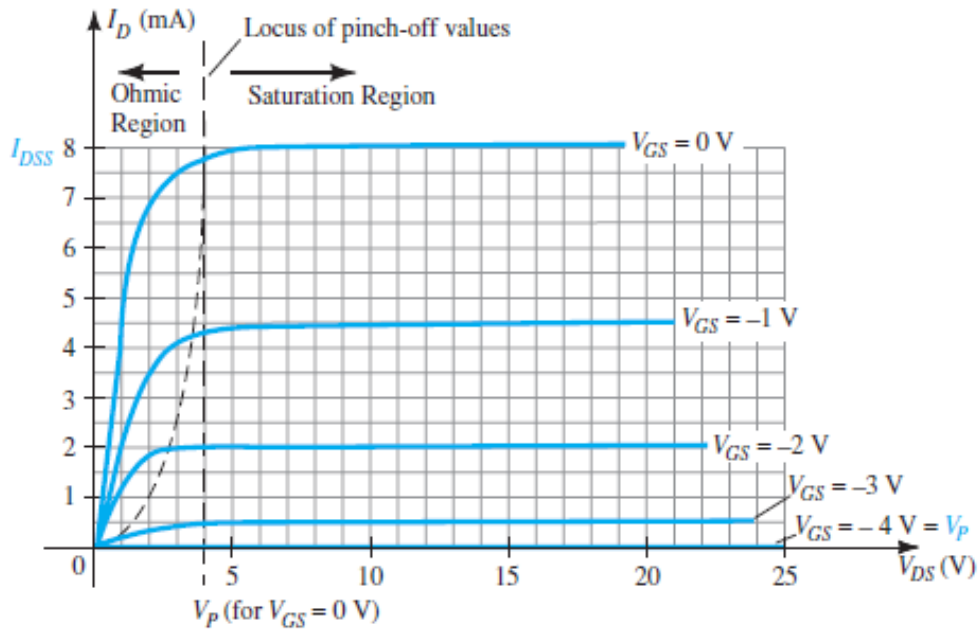
Fig. 8.n- Channel JFET charactristics with I_{DSS}=8mA and V_P=–4 V.

 The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. The pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when V_{GS} = -V_P will be sufficiently negative to establish a saturation level that is essentially 0 mA, and the device has been "turned off."

The level of V_{GS} that results in I_D = 0 mA is defined by V_{GS} =V_P, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.
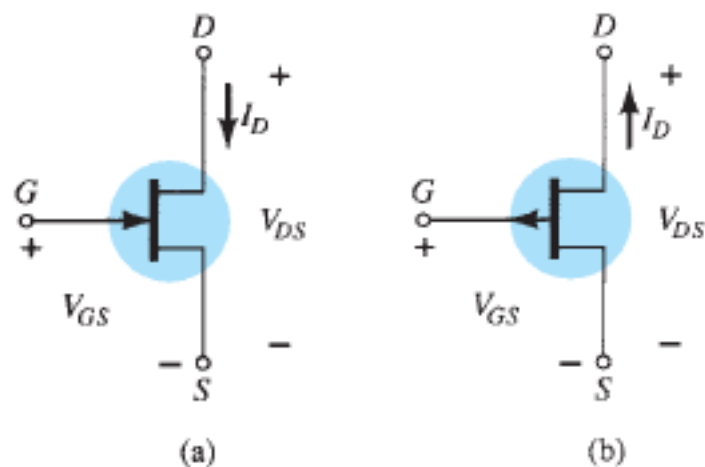

Fig. 9. JFET symbols: (a)n-channel; (b)p-channel.

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2. MOSFET

MOSFET stands for metal – oxide – emiconductor field – effect transistor. MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation.

2.1 DEPLETION-TYPE MOSFET (D-MOSFET)

Basic Construction

The basic construction of the n -channel depletion-type MOSFET is provided in Fig. 10. A slab of p -type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled SS , resulting in a four-terminal device. The source and drain terminals are connected through metallic contacts to n -doped regions linked by an n -channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the n -channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric* , which sets up opposing (as indicated by the prefix *di* -) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

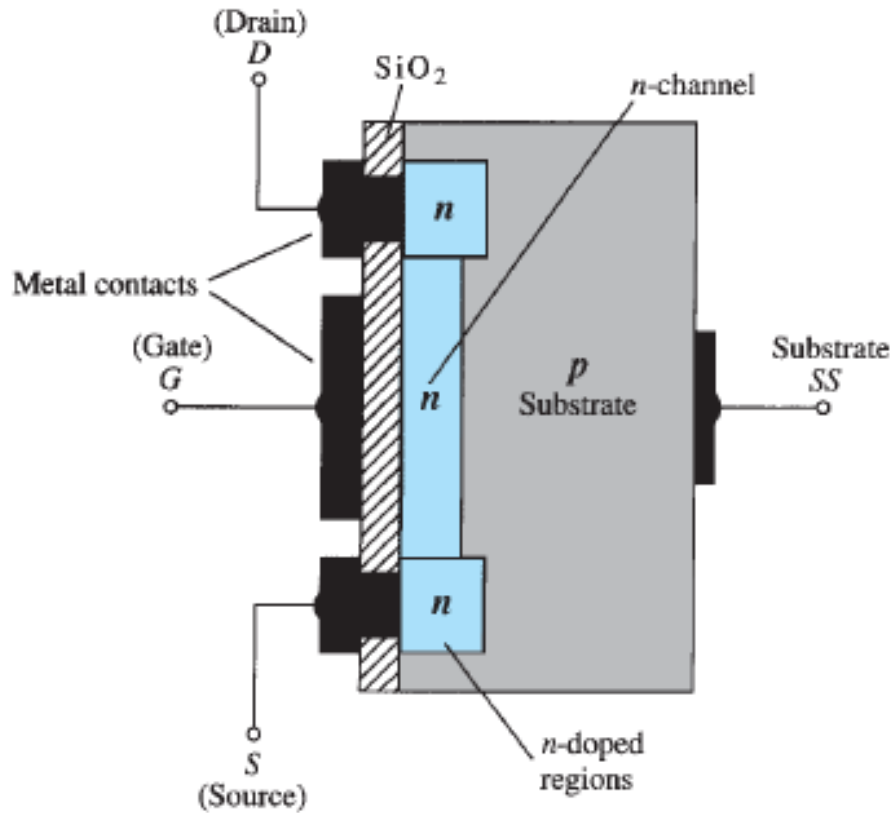*There is no direct electrical connection between the gate terminal and the channel of a MOSFET.*

Fig.10. n-Channel depletion type MOSFET.

In addition:

It is the insulating layer of SiO 2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

The reason for the label metal–oxide–semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections; *oxide* for the silicon dioxide insulating layer; and *semiconductor* for the basic structure on which the *n* - and *p* -type regions are diffused.

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Basic Operation and Characteristics

In Fig. 11, the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the n-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 12.
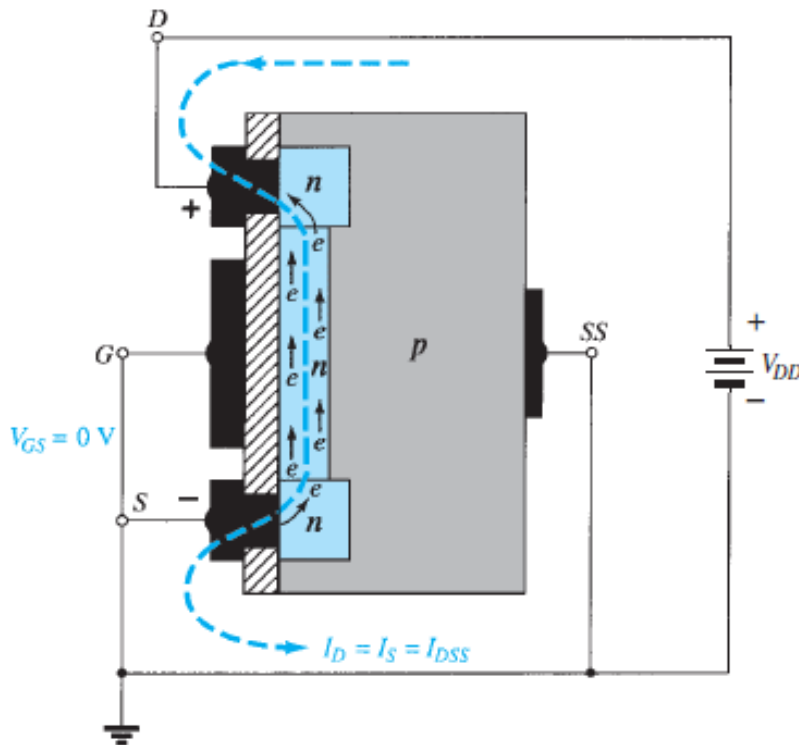

Fig. 11. N-channel depletion type MOSFET with V_{GS}=0V and applied voltage $V_{DD.}$

In Fig. 12, V_{GS} is set at a negative voltage such as –1 V. The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate (opposite charges attract) as shown in Fig. 12. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n -channel available forconduction. The more negative the bias, the higher is the rate of recombination.
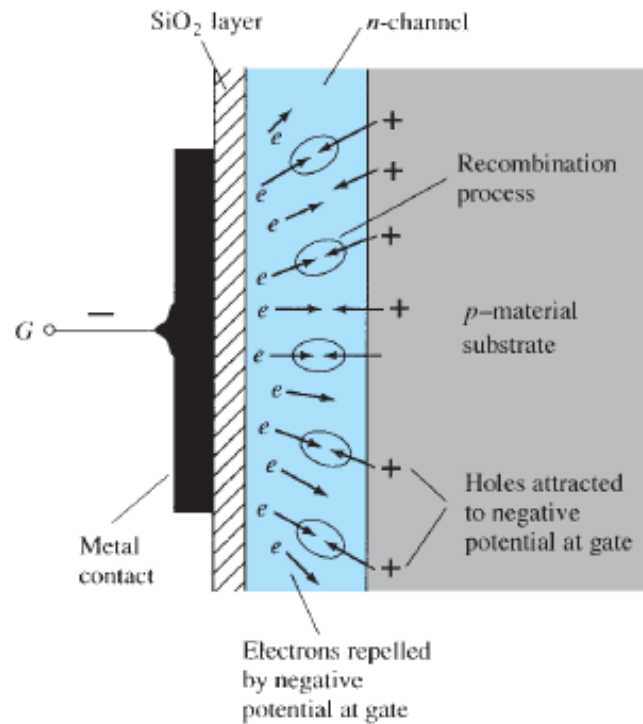
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Fig. 12. Reduction in free carriers in a channel due to a negative potential at the gate terminal.

The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 13 for $V_{GS} = $ -1 V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.
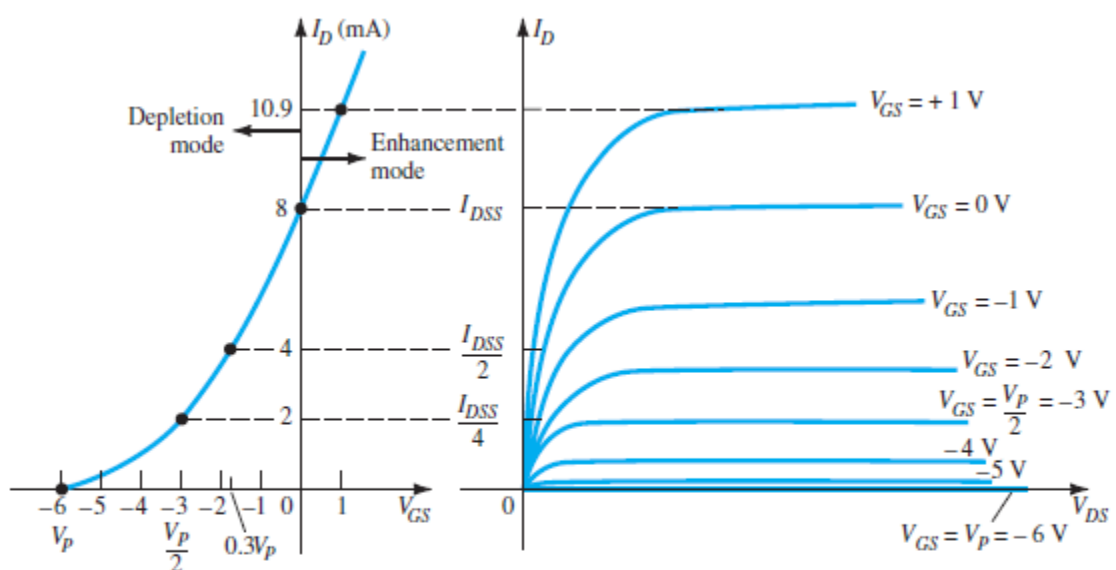

Fig. 13. Drain and transfer characteristics for an n-channel depletion type MOSFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the p -type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig.13 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the V_{GS} =0 V and V_{GS} = +1 V curves of Fig. 13 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 13, the application of a voltage V_{GS} = +4 V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with V_{GS} = 0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region* , with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

2.2 ENHANCEMENT-TYPE MOSFET

Basic Construction

The basic construction of the n -channel enhancement-type MOSFET is provided in Fig. 14 . A slab of p -type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labeled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n -doped regions, but in Fig. 6.32 the absence of a channel between the two n -doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material. Therefore, we can say that the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.
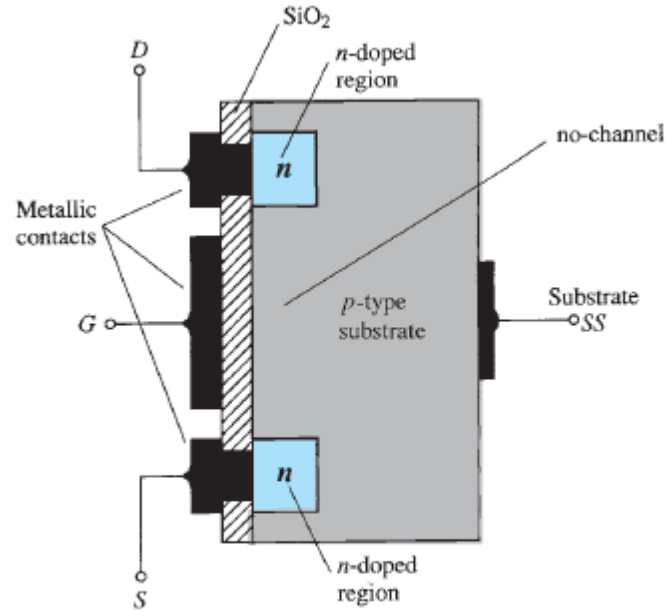
Fig. 14. n-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device of Fig. 14 , the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0 A, wheras in case of JFET and MOSFET $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the n doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased $p -n$ junctions between the n -doped regions and the p -substrate to oppose any significant flow between drain and source.

In Fig. 15, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.
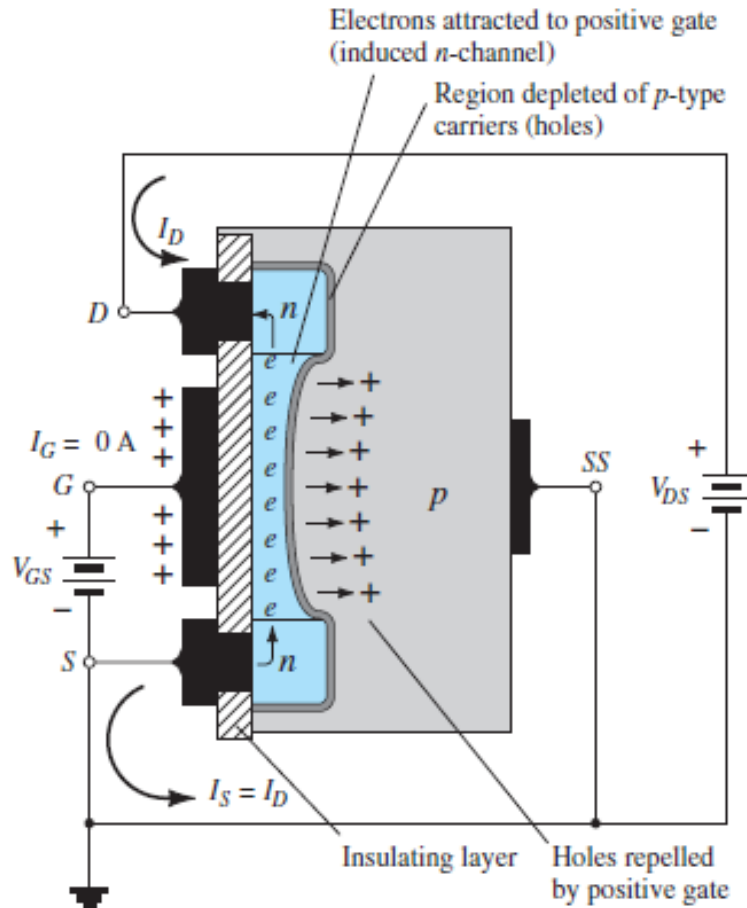
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Fig. 15. Channel formation in the n-channel enhancement-type MOSFET.

The positive potential at the gate will pressure the holes (since like charges repel) in the p - substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p - substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T . On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} =0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion- and enhancement-type MOSFETs have

enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 16.
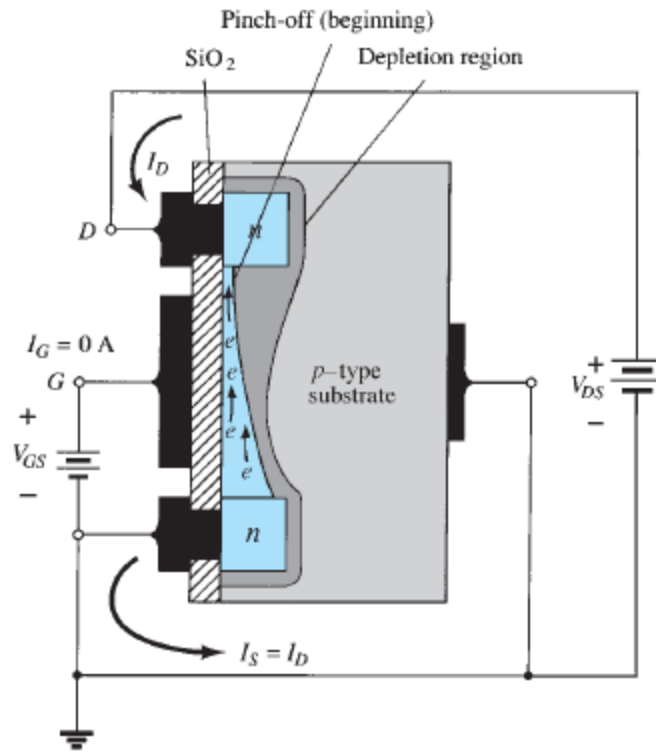
Fig.16. Change in channel and depletion region with increasing level of V_{DS} for a fixed value of $V_{GS.}$

Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 16., we find that

$$V_{DG} = V_{DS} - V_{GS} \qquad (1)$$

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 V to 5 V, the voltage V_{DG} (by Eq.(1)) will increase from –6 V to –3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point

of pinch-off and a saturation condition will be established as happen in the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

The drain characteristics of Fig. 17 reveal that for the device of Fig. 14 with $V_{GS} = 8$ V, saturation occurs at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{sat}} = V_{GS} - V_T \qquad (2)$$

Obviously, therefore, for a fixed value of V_T , the higher the level of V_{GS} , the greater is the saturation level for V_{DS} , as shown in Fig. 14 by the locus of saturation levels.
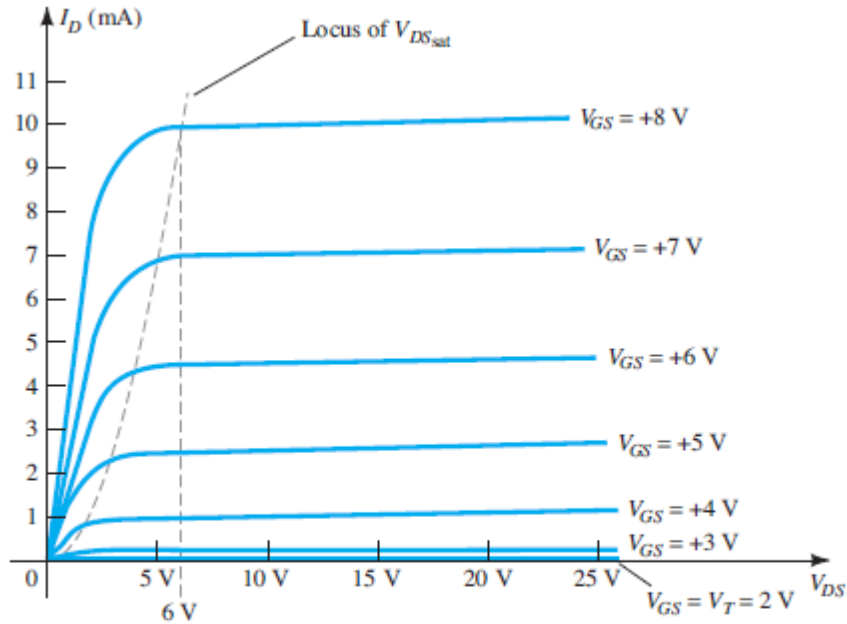

Fig. 17. Drain characteristics of an n-channel enhancement-type MOSFET with $V_T = 2$V and
$$k = 0.278 \times 10^{-3} \ A/V^2$$

For values of V GS less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 17 clearly reveals that as the level of V_{GS} increases from V_T to 8 V, the resulting saturation level for I_D also increases from a level of 0 mA to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increases as the magnitude of V_{GS} increases, resulting in ever-increasing increments in drain current. For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k\left(V_{GS} - V_T\right)^2 \qquad (3)$$

The equation (3) shows a nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the equation (4),where $I_{D_{on}}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

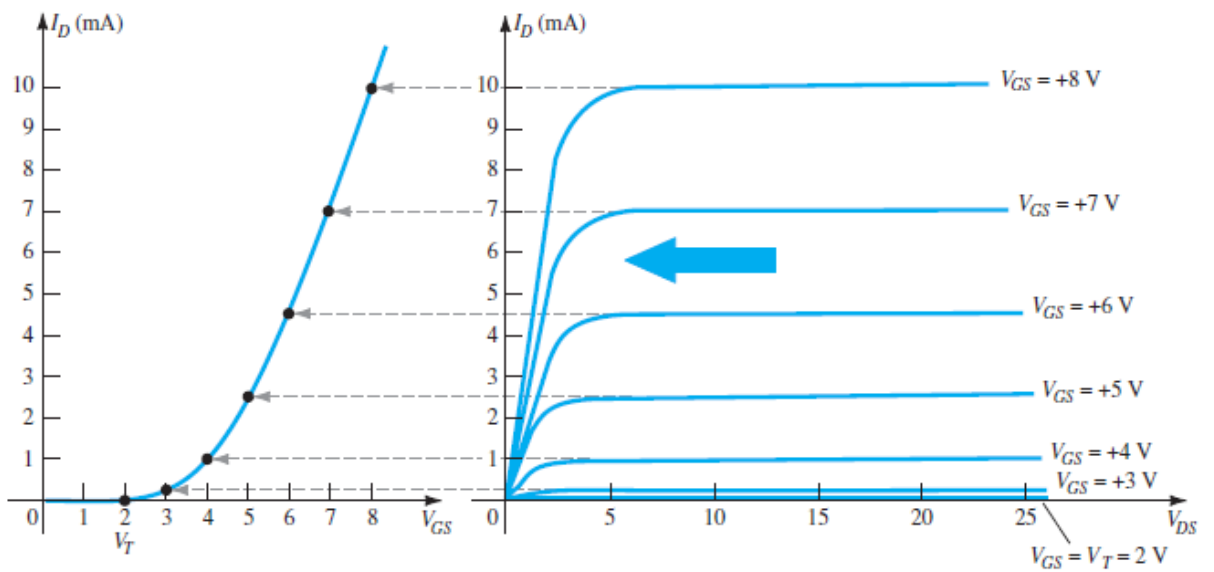$$k = \frac{I_{D_{on}}}{\left(V_{GS(on)} - V_T\right)^2} \qquad (4)$$

Fig. 18. Sketching the transfer characteristics for an n- channel enhancement-type MOSFET from the drain characteristics.

CMOS

A very effective logic circuit can be established by constructing a p-channel and an n-channel MOSFET on the same substrate as shown in Fig. 1. The induced p-channel on the left and the induced n-channel on the right for the p- and n-channel devices, respectively. The configuration is referred to as a complementary MOSFET or CMOS. It is mostly used as an inverter in digital circuits. as shown in Fig. 2 .

An inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa.

In Fig. 2 both gates are connected to the applied signal and both drain to the output V_o. The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, whereas the source of the n-channel MOSFET (Q_1) is connected to ground.

For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V
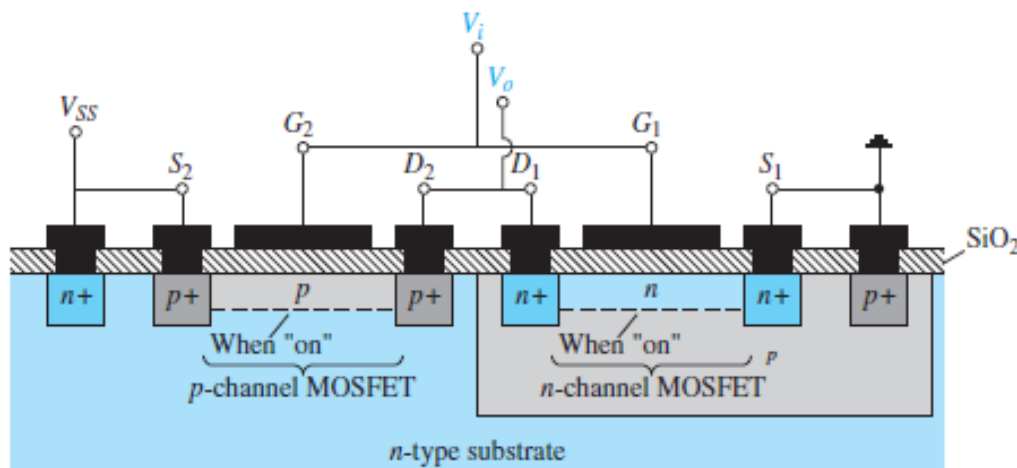

Fig. 1. CMOS with applied voltage to different terminal.

at the output. With 5 V at V_i (with respect to ground), $V_{GS1} = V_i$, and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 3 . Since Vi and V_{SS} are at 5 V, $V_{GS2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2 , as shown in Fig. 3 . A simple application of the voltage-divider rule will reveal that Vo is

very close to 0 V, or the 0-state, establishing the desired inversion process.

For an applied voltage V_i of 0 V (0-state), $V_{GS1} = 0$ V, and Q_1 will be "off" with V_{SS2} = -5 V, turning on the p -channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state).

The CMOS have high input impedance, fast switching speeds, and lower operating power levels.
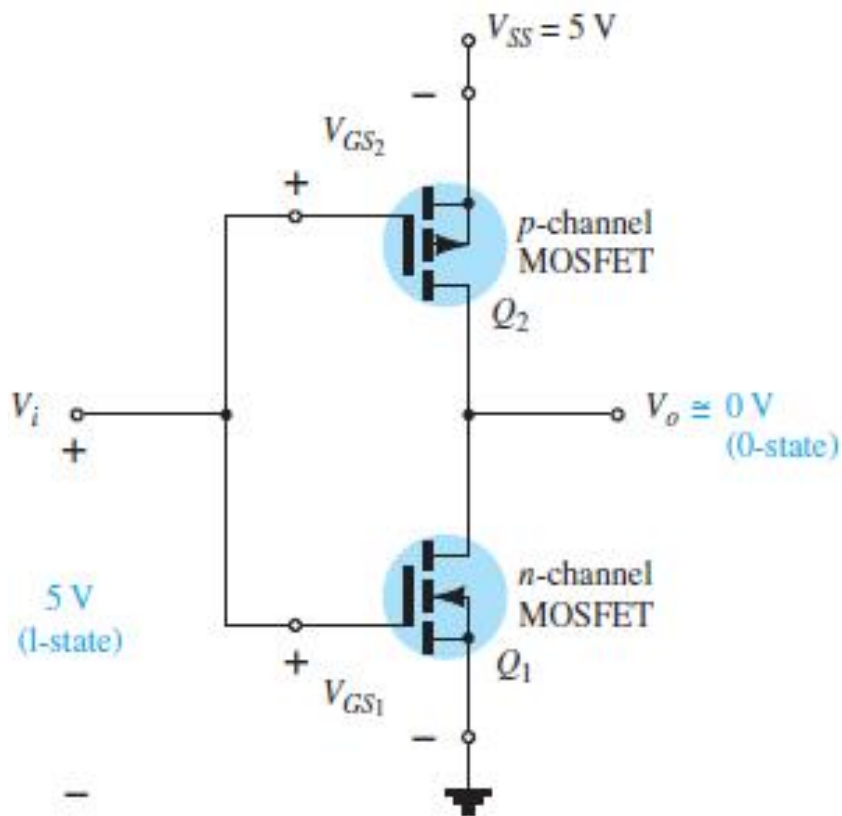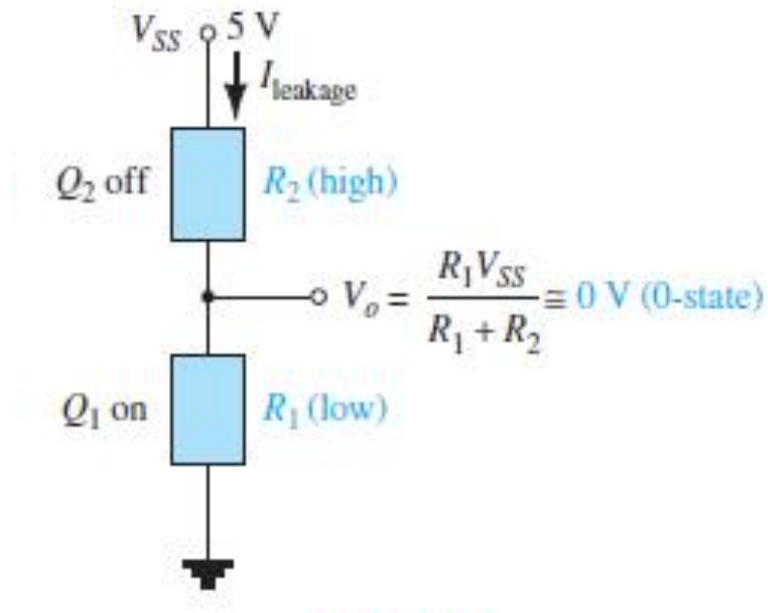

Fig. 2. CMOS inverter.

Fig. 3. Relative resistance level for $V_i = 5$ V (1-State)

Voltage Transfer Characteristics of CMOS

The voltage transfer characteristics of CMOS is shown in Fig. 4. When the input of the driver transistor is less than threshold voltage V_{TH} ($V_{in} < V_{TH}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the V_{DD}. Now, when the input voltage increases further, driver transistor will start conducting the non-zero current and nMOSFET goes in saturation region. Increasing the input voltage further, driver transistor will enter into the linear region and output of the driver transistor decreases.
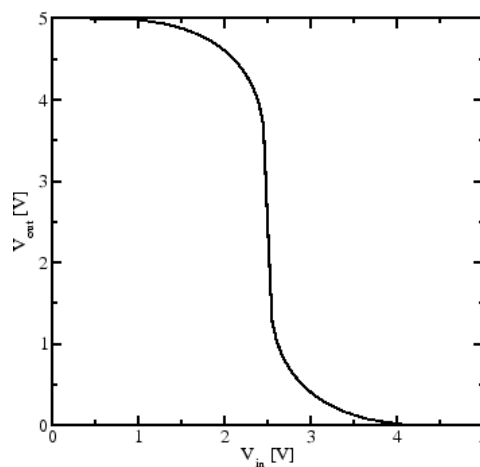

Fig.4. VTC of CMOS.